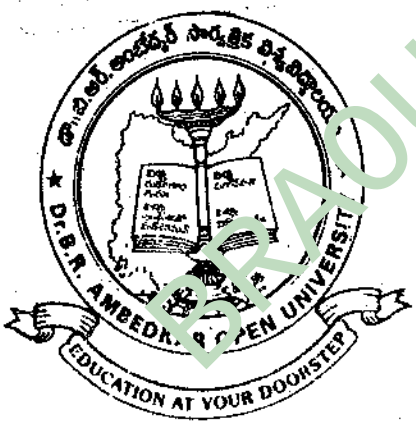
PHYSICS

ELECTRONICS



"We may forgo material benefits of civilization, but we cannot forgo our right and opportunity to reap the benefits of the highest education to the fullest extent ..."

-Dr.B.R. Ambedkar

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Hyderabad
2003

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PREFACE

The book deals with topics in Electronics, a course included in the syllabus of the B.Sc., programme offered by Dr. B.R. Ambedker Open University. The topics cover the advanced area of the subject to be studied in the third year of the three-year degree B.Sc. Course. For the sake of Convenience the syllabus is divided into Eight Blocks, each of which comprises of a number of Units. Each unit generally covers a specific area of the subject. The units are prepared by specialists in accordance with a format so designed as to enable the students to read and understand them selves without much difficulty. Each Unit begins with a statement of its aims followed by the objectives to be achieved after going through these units. At the end of every unit the assignments are given to test the students comprehension in the subject matter. Generally technical terms with which the student may not be familiar are given at the end of each block under the head glossary.

The text is included to be an introduction to the broad field of electronics focusing on some of the most important concepts, devices, circuits and applications. The objective is to take the beginner students to the point where they can effectively use of the concepts learnt by them in the design of simple analog and digital systems.

The subject of electronics is such a fast changing field, which requires updating the knowledge every few years in order to keep up with the rapid developments taking place. Hence, sincere attempt has been made by the authors to revise the book in tune with the developmental trends in the field. Several units have been thoroughly revised by incorporating additional information to the extent necessary and several other units have been revised. In addition, several new units have been incorporated which are essential .

The author's hope that this course material will help the students to get acquainted with the concepts, principles mathematical background and applications of electronics.

Block one deals with semiconductor physics, devices and circuits, block two deals with amplifiers and feed back techniques. Block three deals with the operational amplifiers and applications block four deals with the sinusoidal oscillators and multivibrators. Block five deals with rectifiers, power supplies and regulations. Block six deals with general purposes test and measuring instruments like analog and digital instruments and cathode ray oscilloscope and applications.

Block seven deals with modern communication aspects like Amplitude modulation and detection, Frequency and detection, Radio transmission and reception and TV transmission and reception. Block eight deals with the binary, octal, hexadecimal number systems, digital electronics and Boolean algebra used in modern digital computers. Now a days every modern gadget whether it is a laboratory equipment or industrial unit, or bio-medical equipment, even home appliances are equipped with microprocessor and microcontroller. Hence, a basic course on microprocessors has also been newly incorporated into the subject to expose the students of electronics to these concepts, architecture, programming and applications of microprocessor.

Contents

BLOCK – I

SEMICONDUCTORS

UNIT -1: PHYSICS OF SEMICONDUCTORS

Contents:

1.0 AIMS AND OBJECTIVES

This unit introduces you to the electronic structure of elements, electronic energy levels in atoms and the classification of materials into Insulators, Semiconductors and Conductors based on the energy band theory. Also introduces you to the concept of Intrinsic and Extrinsic of semiconductors. This unit explains the basics of the

1) Electronic Energy Levels in an isolated atom and energy bands in an atom bound in a crystal lattice
2) Physics of Semiconductors
3) Intrinsic Semiconductors
4) Extrinsic Semiconductors

While understanding these concepts you will be able to explain the different processes of electrical conduction in semiconductors

1.1 INTRODUCTION

From the early days of the Second world war until 1960's revolutionary changes have taken place in Semiconductor Technology and hence in the field of electronics. In order to understand the developments in electronics, it is essential that one should know the physics of semiconductors to analyse their behaviour under different physical conditions.

For each integral value of n in Equ (1.1) a horizontal line is drawn. These lines are arranged vertically in accordance with the numerical values calculated from Equ. (1-1). Such a convenient pictorial representation is called an energy-level diagram and is indicated in Fig. 1-1 for hydrogen. The number to the left of each line gives the energy of this level in electron volts. The number immediately to the right of a line is the value of n. Theoretically, an infinite number of levels exist for each atom, but only the first five and the level for n = ∞ are indicated in Fig. 1-1.

The energy levels of each state in an atom are found with the help of Equ. (1.1).

$$W_{joules} = -\frac{m_q^4}{8h^2\varepsilon_o^2} \cdot \frac{1}{n^2} \qquad \ldots(1.1)$$

Where

m - is its mass of electron
q – is the electron charge
ε_0 - Permitivity of free space
h – Plank's constant

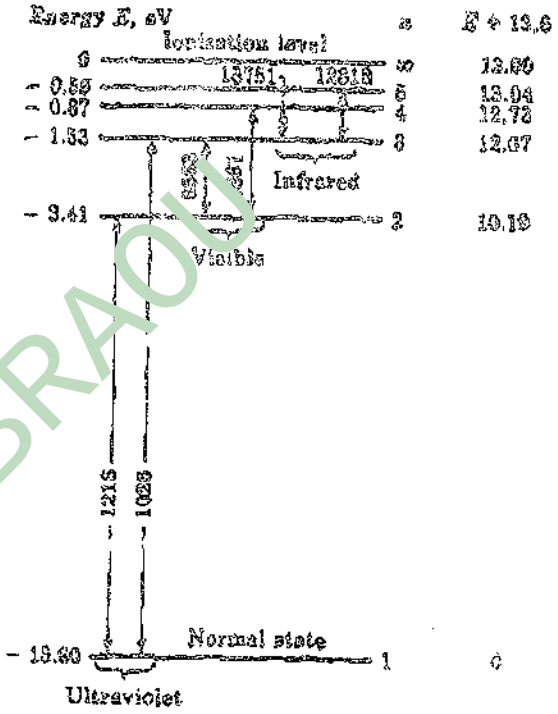


Fig 1.1 The lowest five energy levels and the ionization level of hydrogen. The spectral lines are in angstrom units

The horizontal axis has no significance here, but in extending such energy-level diagrams to solids, the X-axis will be used to represent the separation of atoms within a crystal (Fig. 1-2) or the distance within a solid. In such cases the energy levels are not constant, but rather are functions of x.

It is customary to express the energy value of the stationary states in electron volts eV rather than in joules(W). Also, it is more common to specify the emitted radiation by its wavelength λ in angstroms rather than by its frequency f in hertz. In these units, Equ.(1.1) may be rewritten in the form.

$$f = \frac{W_2 - W_1}{h} \qquad \ldots(1.2)$$

$$\lambda = \frac{12,400}{E_2 - E_1} \qquad \ldots(1.3)$$

Where f – is the frequency

λ - wavelength of radiation

Since only differences of energy enter into this expression, the zero state may be chosen at will. It is convenient and customary to choose the lowest energy state as the zero level. Such a normalized scale is indicated to the extreme right in Fig. 1-1. The lowest energy state is called the normal, or ground, level, and the other stationary states of the atom are called excited, radiating, critical, or resonance, levels.

As the electron is given more and more energy, it moves into stationary states, which are farther, and farther away from the nucleus. When its energy is large enough to move it completely out of the field of influence of the ion, it becomes "detached" from it. The energy required for this process to occur is called the ionization potential and is represented as the highest state in the energy-level diagram, 13.60 eV for hydrogen Etc.

Collisions of Electrons with Atoms The foregoing discussion shows that energy must be supplied to an atom in order to excite or ionize the atom. One of the most important ways to supply this energy is by electron impact. Suppose that an electron is accelerated by the potential applied to a discharge tube. The energy gained from the field may then be transferred to an atom when the electron collides with the atom. If the bombarding electron has gained more than the requisite energy from the discharge to raise the atom from its normal state to a particular resonance level, the amount of energy in excess of that required for excitation will be retained by the incident electron as kinetic energy after the collision.

If an impinging electron possesses an amount of energy at least equal to the ionization potential of the gas, it may deliver this energy to an electron of the atom and completely remove it from the parent atom. Three charged particles result from such an ionizing collision: two electrons and a positive ion.

1.3 ELECTRONIC CONFIGURATION AND ENERGY BAND STRUCTURE OF MATTER

Consider the four elements Carbon (C), Silicon (Si), Germanium (Ge) and Tin (Sn) whose electronic configurations are shown in Table 1.1

Table I

Element	Atomic Number	Electronic Configuration
C	6	$1S^2\ 2S^2\ 2p^2$
Si	14	$1S^2\ 2S^2\ 2p^6\ 3S^2\ 3p^2$
Ge	32	$1S^2\ 2S^2\ 2p^6\ 3S^2\ 3p^6\ 3d^{10}\ 4S^2\ 4P^2$.
Sn	50	$1S^2\ 2S^2\ 2p^6\ 3S^2\ 3p^6\ 3d^{10} 4S^2\ 4p^6 4d^{10} 5S^2\ 5p^2$

Each of these elements shown in table 1.1 has completely filled subshells except for the outermost p-shell, which contains only two of the six possible p-electrons. Though they are similar as far as this property is concerned, carbon in the diamond form behaves like a good insulator, Silicon and Germanium as semiconductors and tin as a good conductor. This can be explained on the basis of band theory of sol ids when the atoms form crystals such as diamond it is found that the energy levels of the inner shell electron is not affected appreciably by the presence of the neighbouring atoms. However, in the case of Si, Ge the levels of the outshell electrons are changed considerably, since these electrons are shared by more than one atom in the crystals. It is found that coupling

between the outer shell electrons of the aroms results in a band of closely spaced energy states.

Consider a crystal consisting of N atoms of one of the elements mentioned in Table 1 Imagine that it is possible to vary the spacing between the atoms without altering the type of fundamental crystal structure. The outer two subshell for each element contain two 's' electrons and two 'p' electrons if we ignore the inner shell levels, there are 2N electrons completely filling the 2N possible 's' levels all at the same energy. Since the p atomic subshell has six possible states the rest of 2N electrons fill only 2N states of 6 N possible 'p' states at the same level as shown in Fig 1. 2 (a)

If we now decrease the inner atomic spacing, an atom will exert an electronic force on its neighbours, then the 8N energy levels are separated forming into a closely spaced energy levels called an energy band as shown in Fig 1.2 (a) The 2N states in this lower part of the energy band are occupied completely by 2N electrons and out of 6N states of the upper part of the energy band only 2N are completely filled by electrons. There is an energy gap (which is known as forbidden energy band) between the two bands discussed above, which decreases as the atomic spacing decreases. For smaller enough distances as shown in Fig. 1.2 (a) these bands will overlap. Now the 6N upper states merge with the 2N lower states giving a total of 8N levels. Out of 8N energy levels, 4N levels are completely filled by the available electrons. Thus each atom has given up 4 electrons to the band. These electrons can no longer be said to orbit in s or p subshells of an isolated atom but they belong to a crystal as a whole. This band is known as valence band since; the four valence electrons of the atoms occupy this band.

If the spacing between the atoms is still decreased below the distance at which the bands overlap, we can expect energy band diagrams as noted in Fig 1.2 (C). At the crystal lattice spacing (the dashed vertical line) we find the valence band filled with 4N electrons separated by a forbidden band (no allowed energy states) of extent EG from an empty band 4N additional states exist in this band. This upper vacant band is known as conduction band.

1.3.1 Insulator:

A poor conductor of electricity is known as an insulator, a good conductor is known as a metal and substance whose conductivity lies between these extremes is known as a semiconductor. The energy band structure of fig 1.2 (a) is shown for an Insulator: Such as diamond crystalline Carbon the width of the forbidden energy gap is around 6~7eV as in Fig1.1 (b) for a semiconductor with an energy gap of 0.7 – 1.2 eV and for a conductor (overlapping bands). The energy gap is indicated in Fig. 1-2(C) widely separates the filled valence band from the vacant conduction band. The conduction is impossible since the energy supplied to the electron from an applied field is not sufficient to carry the electron from the filled valence band to the vacant conduction band. Hence diamond behaves as an insulator.

1.3.2 Semiconductor:

A substance for which the width of the forbidden energy gap between the condition band and valance band is around 1.0 eV is called a semiconductor. In Germanium and Silicon the width of this gap are 0.785 and 1.21 eV respectively at zero degree Kelvin as in Fig 1.2c(ii). At very low temperatures, these substances behave as insulators. But as the temperature is increased some of these valence electrons acquire thermal energy greater than E_G (width of the forbidden energy gap) and hence move into the conduction band. Now these free electrons can move about freely under the influence of a small electric field. Hence it is known as a semi conductor.

1.3.3 Conductor:

The band structure may not contain forbidden energy region so that the valence band merge into the conduction band as in Fig 1.2(C) (iii), Under the influence of an applied field, the electrons acquire additional energy and can jump into higher energy states, Since these free electrons constitute a current such substances are called conductors. A metal consists of overlapping of valence and conduction band.

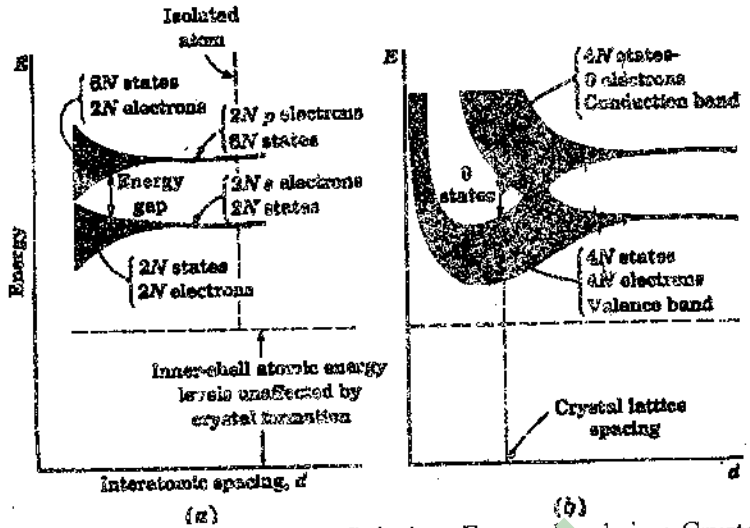


Fig 1.2 Energy Levels of Isolated atom Split into Energy bands in a Crystal Lattice

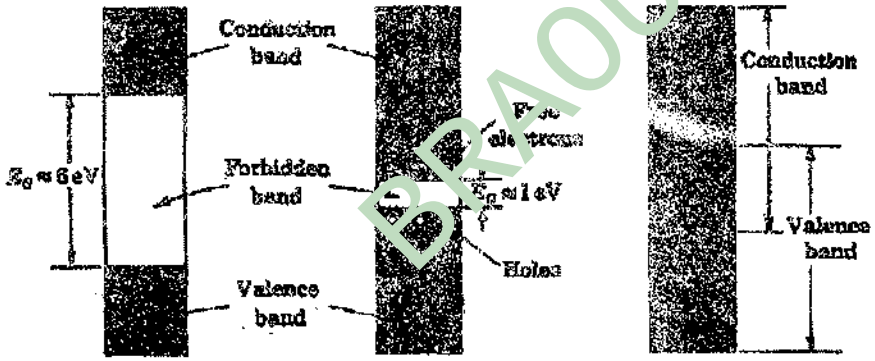


Fig1.2 (c) Energy Band Structure:

1.4 INTRINSIC OR PURE SEMICONDUCTORS

There is a sharp demarcation between insulators and conductors. There is yet another category of materials which are neither perfect insulators nor good conductors; they are called semiconductors. These are characterised by small energy gaps of the order of 0.7 to 1.2eV. Most widely used elemental semiconductor materials are germanium and silicon.

An atom of germanium has a total number of 32 electrons, and its electronic shell configuration is: $1s^2\ 2S^2\ 2p^6\ 3S^2\ 3p^6\ 3d^{10}\ 4S^2\ 4P^2$. The fourth shell is incomplete and so it is the valence shell. In order to be complete it requires either to acquire 4 electrons into 4p sub-shell or it should loose 4 electrons from 4p and 4s sub-shells. In either of these cases, gaining or lossing involves the same number of electrons; therefore, exactly the same energy change is involved.

The Germanium and Silicon atoms are arranged in a crystal lattice. No adjacent atoms enter into sharing of electrons. This is a unique character of the elements like carbon, silicon, germanium etc. A sharing of two electrons between any two adjacent atoms is said to constitute a covalent bond. Each germanium atom takes part in four covalent bonds. As a consequence of this covalent bonding, the atoms arrange themselves in a tetrahedral arrangement as shown in Fig. 1.3.

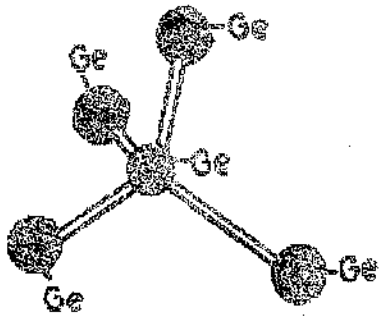


Fig. 1.3 Tetrahedral arrangement of germanium or silicon atoms
Ge = germanium

To facilitate the explanation the atomic arrangement is shown in a schematic way in Fig. 1.4. In a real situation the atoms in a crystal are not stationary as dipicted in figure but they would be vibrating about an average position as the temperature of the crystal is raised the rapidity of the motion of the atoms also increases. The positions of the atoms shown in Figs. 1.4 and 1.5 depict the average positions only.

The situation is very much the same in the case of silicon atoms also. Its valence shell is filled with four electrons leaving a room for four more electrons. Hence silicon atoms form covalent bonds and the structural arrangement of atoms is similar to that of germanium.

At this stage either germanium or silicon crystals would behave as insulators as there are no free electrons (charge carriers). However, even at room temperature the violent vibrations of the atoms is enough to break some of the covalent bonds and release the electrons. While in the bond the electron has an energy corresponding to the valence band once it is free upon breaking of a covalent bond, the electron energy corresponds to that of conduction band.

Each atom before it takes part in covalent bonding had exactly same magnitude of positive charge in its nucleus and equal amount of negative charge carried by its electrons that revolve round the nucleus. This makes the atoms electrically neutral. Fig 1.5 shows a two-dimensional, simplified version of a semiconductor in which the electrons that are held in covalent bonds are indicated.

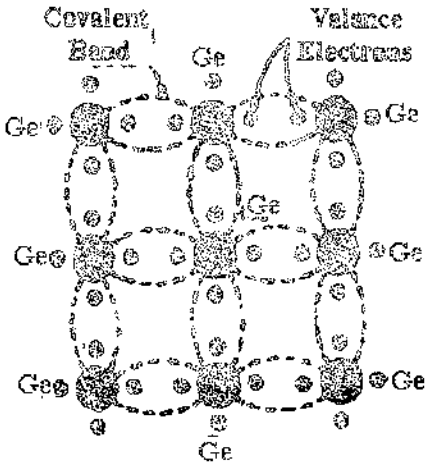


Fig. 1.4 Schematic representation of Intrinsic semiconductor crystal.

In this schematic representation the nucleus and the inner completed shells of each atom are combined into one unit called the core.The cores of either germanium or silicon has a net charge of + 4 units. This core along with four valence electrons, each one appearing in four corresponding covalent bonds constitutes a neutral atom. When the thermal energy that electrons receive at room temperature is sufficiently large to enable some of the electrons to break the covalent bonds and become free electrons for conduction. When such an electron leaves the shell it leaves behind a gap into which another electron can move and such a gap is termed a Positive by charged hole. In semiconductor terminology, the absence of an electron in a covalent bond is known as hole. Thus breaking of a covalent bond not only liberates an electron but also it leaves behind a positively by charged hole thus an electron-hole pair is formed. In intrinsic semiconductors the number of free electrons is exactly equal to the number of holes produced as shown in Fig 1.5(a).

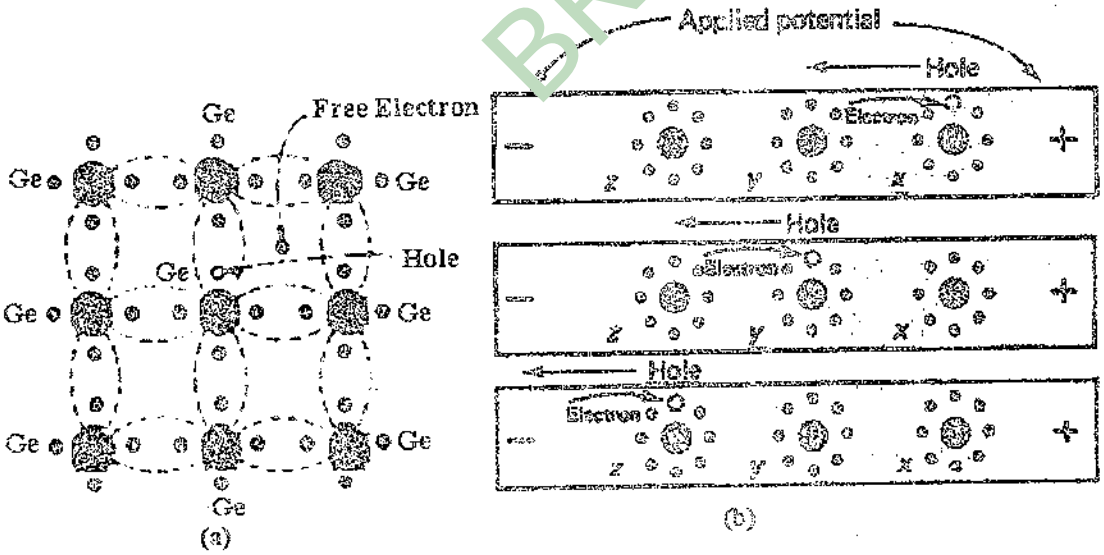


Fig.1.5 (a) Schematic representation of intrinsic semi- conductor crystal. Thermally Broken Covalent Bond and (b) Hole Conduction

At room temperature approximately one out of 10^{13} bonds in germanium and one out of 10^{10} bonds in silicon are broken on an average. Now let us examine what happens inside an intrinsic semiconductor upon the application of voltage to it. The negatively charged free electrons are attracted towards the positive and an electric current sets in. The applied electric field acts not only on electrons but also on positively charged holes. As discussed earlier the electric filed acting on the holes cannot make the hole to move from its position but at the most it can cause a bound electron from the adjacent, bond to

move into the hole.

This in a way, results in shifting of the hole from one position to the other towards the negative electrode. This shift causes the transport of a hole along with its positive charge as shown in Fig 1.5(b) if the electric field is directed from left to right.

The hole will successively move towards the negative electrode. However, it is difficult at first to accept this hole motion. When we say that a hole has moved, it is actually a series of various bound electrons that move from one bond to the other in the opposite direction i.e., towards the positive electrode. The, electrons that participate in hole conduction are essentially bound electrons and not the free electrons. The hole will successively move towards the negative electrode. However, it is difficult at first to accept this hole motion.

When we say that a hole has moved, it is actually a series of various bound electrons that move from one bond to the other in the opposite direction i.e., towards the positive electrode. The, electrons that participate in hole conduction are essentially bound electrons and not the free electrons. This discussion makes it clear that the electrons in a semiconductor are highly mobile than the corresponding holes. In fact in a semiconductor the mobility of electrons is more compared to the mobility of holes. We now see that the current flow in a semiconductor results from the motion of two distinct charges, namely negatively charged electrons and positively charged holes. This explains why the resistance of a semiconductor decreases with increase in temperature that is as the temperature increases more and more number of covalent bonds break down and more charge carriers are created thereby causing the electrical resistance to decrease.

There are two main limitations in using the pure semiconductors. Firstly the total number of charge carriers -available to conduct an- electric current is relatively low (hence the name semiconductors) and secondly the free electrons may recombine with the holes. (Electron-hole recombination process) hence most of the useful charge carriers are lost in this process. Thus the current through a pure (intrinsic) semiconductor is practically zero or negligibly small.

1.5 EXTRINSIC OR IMPURITY DOPED SEMICONDUCTORS

1.5.1 Doping of Semiconductors:

Conduction in semiconductor materials can be greatly enhanced by the addition of certain chosen impurities in precisely controlled quantities. This process is called doping. The substances resulting from this impurity doping are called "impure or extrinsic semiconductors".

The conduction process involved in doped semiconductors is called impurity conduction or extrinsic conduction. Two types of semiconductor materials can be formed through controlled addition of appropriate impurities. In one type of semiconductors called n-type, conduction results mainly due to electron flow while in the other type, known as p-type, conduction results from hole motion.

1.5.2 p- Type Semiconductor:

p-type semiconductors are formed by the addition of small quantities (1 part in 10^8) of boron, aluminium, gallium or indium to the intrinsic semiconductor crystal (either germanium or silicon). These impurity atoms have three electrons in their valence shell. Replacement of germanium atoms by these trivalent impurity atoms in the crystal cannot satisfy all four covalent bonds around them. One covalent bond near- each p-type impurity atoms is incomplete and this shortage of one electron results in the formation of a hole. These trivalent impurity atoms are called acceptors, since they can accept one more electron into its incomplete bond. The situation in a p-type semiconductor is

schematically illustrated in Fig. 1.6

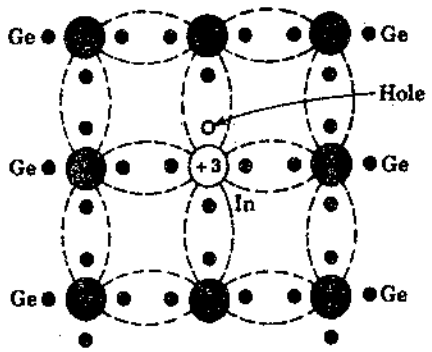


Fig. 1.6 p-type Semi Conductor A.I.-acceptor impurity; Hole Conduction

The term p-type is used to indicate that the major part of the current is carried by holes. Thus the holes are known as majority charge carriers and electrons are the minority charge carriers in the p-type material.

1.5.3 n-type Semiconductor:

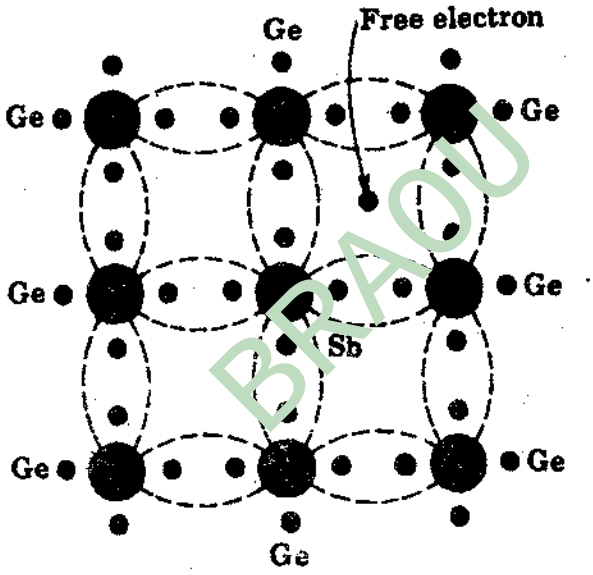


Fig. 1.7. n-type Semi Conductor
DI-Donar Impurity Conduction Electrons

n-type of semiconductors are formed by doping the intrinsic semiconductor with small quantities of (1 in 10^8) of a pentavalent impurity (those elements having five electrons in the valence shell) like phosphorus, arsenic or antimony to the intrinsic semiconductor. The impurity atom replaces one of the germanium atom in the crystal structure. These impurity atoms also form covalent bonds with the surrounding germanium atoms. Each impurity atom contributes one electron to each four covalent bonds, but each impurity atom has one excess electron that does not take part in covalent bond. This excess electron is weakly bound to the core. At room temperature it acquires sufficient energy to be considered as a free electron. This is diagrammatically represented in Fig. 1.6.

Since these impurity (pentavalent) atoms donate one electron each they are called donor atoms or simply donors. The doping of an intrinsic semiconductor with donor impurity increases the population of free electrons without affecting the hole population. The essential characteristic of an n-type semiconductor is therefore the electron

population is more than the population of holes. So the majority charge carriers are electrons, and holes are referred to as the minority charge carriers in an n-type semiconductor. The term n-type, of course, is used to indicate that the major part of the current is carried by electrons.

The terms 'majority' or minority charge carriers have some relevance only if we specify the type of semiconductors, whether it is an n-type or a p-type semiconductor.

1.6 ELECTRICAL CONDUCTION IN SEMICONDUCTORS.

There are two distinct and separate processes involved in semiconductor materials that account for the flow of current. The first process is called drift and the second mechanism is known as diffusion.

1.6.1 Drift of Charge Carriers

For any given material we can measure the current resulting from a known applied voltage. The ratio of the voltage to the current is known as resistance, so

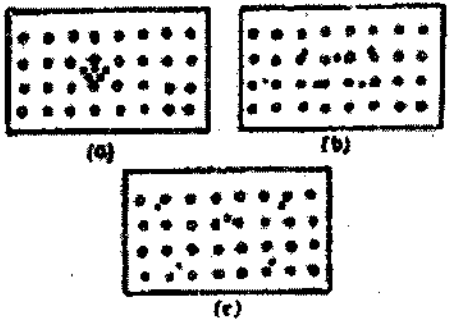
$$\frac{V}{I} = R = \frac{\rho L}{A} \quad \text{or} \quad I_{Drif} \alpha V \qquad \ldots(1.4)$$

Where L is the length of the sample, A is the area of cross-section of the sample and ρ is the resistivity of the material. In semiconductor materials the higher the level of doping, the higher the number of free charge carriers and lower the resistivity. Thus the effect of doping is to lower the resisitivity or increase the conductivity. We can see from Equ. (1.2), the drift current I is proportional to the applied voltage. For the same magnitude of voltage applied to two samples of germanium having identical shape and size, one intrinsic and the other doped, we would expect a larger current in doped or extrinsic semiconductors than in intrinsic semiconductors.

Suppose we apply a potential difference between the ends of a p-type or n-type of semiconductors, both majority as well as the minority charge carriers move (driff) in opposite directions to constitute a net current. We can define drift as the motion of charge carrier under the influence an applied electric field and the net current flows through the semiconductor as drift current.

1.6.2 Diffusion of Charge Carriers

Let us take a glass of water and put a drop of ink and examine. The ink drop slowly diffuses through the water until all the water is evenly coloured by the ink. Almost a similar process occurs in semiconductors. If we take a p-type semiconductor (germanium sample) and in same manner introduce an excess number of electrons into a very small region of the sample, these electrons will slowly diffuse through the sample so as to be evenly distributed throughout the material. The motion of minority charge carries strictly follows a statistical phenomena and not the result of any coulomb attraction or repulsion. Diffusion usually takes place in a direction away from the region of highest density of minority charge carriers. For example, electrons in p-type and holes in n-type usually diffuse into a region of low density of minority charge carriers. In the present case in our example, that is electrons in a p-type are introduced.



(a) Large Electron Connecntration in a Localised area
(b) and (c) electrons diffuese slowly away from the area of highes denity

Fig. 1.8. Phenomenon of Diffusion.

This is schematically represented in Fig. 1.8. Of course, there is always a danger that the majority carriers recombine with the incoming minority carriers and those majority charge carriers are lost for the process of conduction.

1.7 SUMMARY

Materials are classified on the basis of their conductivities as conductors, semiconductors and insulators. Addition of chosen impurities in controlled amounts to intrinsic (pure) semiconductors materials is called doping and results in the formation of doped (extrinsic) semiconductors. Drift and diffusion are two distinct processes in semi conducting materials for movement of charge carriers, which constitute the flow of current.

1.8 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Discuss the electronic energy levels in an isolated atom and energy bands in an atom bound in a crystal lattice
2. Discuss the classification of materials based on their conductivity scale.
3. Characterize conductors, insulators and semiconductors on the basis of their energy gap.
4. Discuss the characteristic structures of intrinsic (pure) and extrinsic (impure) semiconductors. How are p and n type semiconductors formed? Discuss the structure of the p-type and n type semiconductors in detail.

II Answer the following questions briefly

1. What is the importance of Valence shell and Valence electron?
2. Give some examples of materials that are good insulators and state why they are good insulators
3. Describe the electrical conduction in a n-type semiconductor, which carriers are responsible for most of the current, why?
4. Distinguish between majority and minority charge carriers.

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   Donald
5. Integrated Circuits — K.R. Bothkar
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UNIT-2: THE PN JUNCTION: DIODES AND TRANSISTORS

Contents:

2.0 AIMS AND OBJECTIVES

This unit explains the properties of p-n junction diodes, behaviour of different types of diodes and the functioning of bipolar junction transistor.

After going through this unit you will be able to explain

1) The terms depletion layer and contact potential
2) The modes of biasing a diode and the Avalanche and Zener breakdown mechanisms
3) The behaviour of a Zener diode

2.1 INTRODUCTION

The pn junction is the essential building block for a variety of devices. With the introduction of the semiconductor diode, we start our study of semiconductor devices. If one can understand the basic physics of semiconductors, it becomes easy to predict the properties and the behaviour of these devices. The diode has many interesting and useful circuit applications. It should be studied because of its use in such circuits as power supplies, electronic tuning, of VHF circuits, voltage regulation and voltage protection. The term transistor arises from a combination of the italicized portions of the words Transfer and Resistor. The Transistor and other semiconductor devices have brought in phenomenal developments, which have led to the new applications particularly in electronic circuitry. These semiconductor devices have lead to the development of integrated circuits.

2.2 THE PN JUNCTION

2.2.1 Depletion Region and Contact Potential

When p-type and n-type semiconductors are brought together to form a Junction, a very important semiconductor device called diode is obtained. The pn junction is the essential building block for a variety of devices, as we shall see later.

At the junction that is formed, one side (the n-side) has a large population of electrons, whereas the other side (the p-side) has a large population of holes. Electrons from the n-side diffuse across the junction into the p-side and holes from the p-side due to a large electrostatic force exerted by the positively charged p-block diffuse across the junction into the n-side due to large electrostatic force exerted by the negatively charged n-block, as shown In Fig. 2.1. Before they were brought into contact, both sides were electrically neutral. As a result of diffusion, the n-side develops a net positive charge and the p-side develops a net negative charge. This difference is due to the fact that the n-side material lost electrons and gained holes at the same time the p-side lost holes and gained electrons. Even then the diode as a whole is electrically neutral. Since in a diode the net positive charge in n-side must be exactly equal to the net negative charge in the p-region. These charges thus developed (negative charges in the p-side and the positive charges in the n-side) are not free to move. They are stationary because they are bound to the ions in the crystal on either side of the depletion region. The net positive charge in the n-side comes from the donor nuclei, which have lost their fifth electron and the net negative charge in the p-side comes from the accepted nuclei, which have lost their holes.

2.2.2 Diode under no Bias:

The process of diffusion of charge carriers across the junction continues till no additional carriers have sufficient energy to overcome the electric field, which has built up at the junction as a result of the redistribution of charges thus equilibrium is reached.

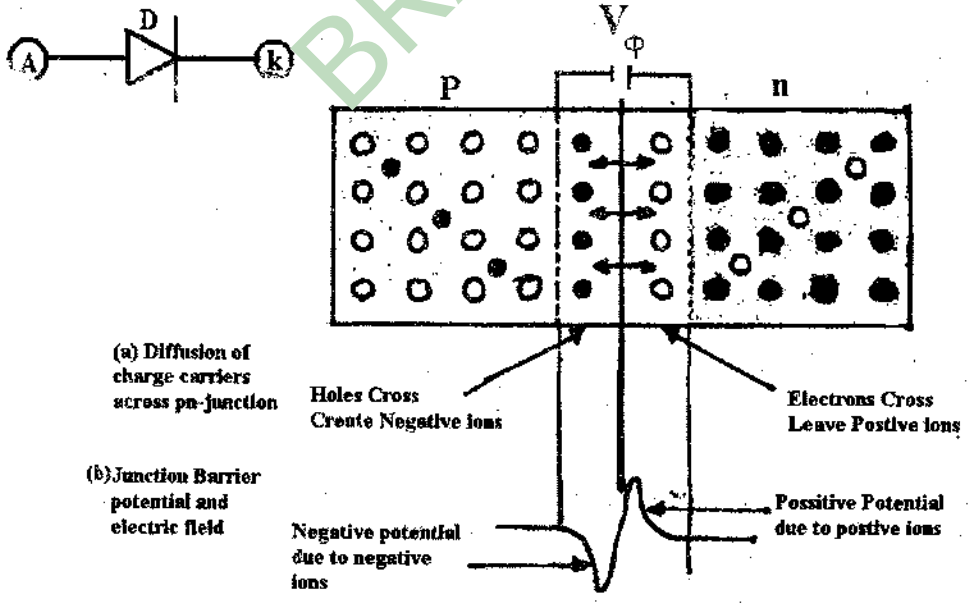


Fig 2.1 Formation of Depletion Region (a) diffusion of charge carries (b)euilibrium state
DR= Depletion Region or space charge region or transition region

This situation is show in Fig. 2.1. The positively charged donor ions in the n-side repel holes, while the negatively charged acceptor ions in the p-side repel electrons. The region on either side of the junction where the stationary charges appear is called the depletion region. The name comes due to the fact that this region has been depleted of all mobile charge carriers. This region is also called space-charge region.

An Electric field acting over the width of the depletion region causes a potential difference between the p and n regions. This difference in potential is usually called the contact potential or cut-in potential V_ϕ. The magnitude of the contact potential depends not only on the doping concentrations in the n and p regions but also on the type of semiconductor material (germanium or silicon) used. The diode under equilibrium conditions without any externally applied bias voltage is shown in Fig. 2.1 along with the diode circuit symbol.

2.3 BEHAVIOUR OF A PN JUNCTION DIODE UNDER BIAS

Now let us examine the action of the diode when Fig. 2.2. pn Junction diode is biased an (external-field is applied). (a) If the positive terminal of a battery is connected to the p-side (called the anode) and the negative terminal of the battery is connected to the n-side (called the cathode) a fairly high current flows through the circuit. In this condition the diode is said to be forward biased (as shown in Fig. 2.2a) and the current is called forward current.

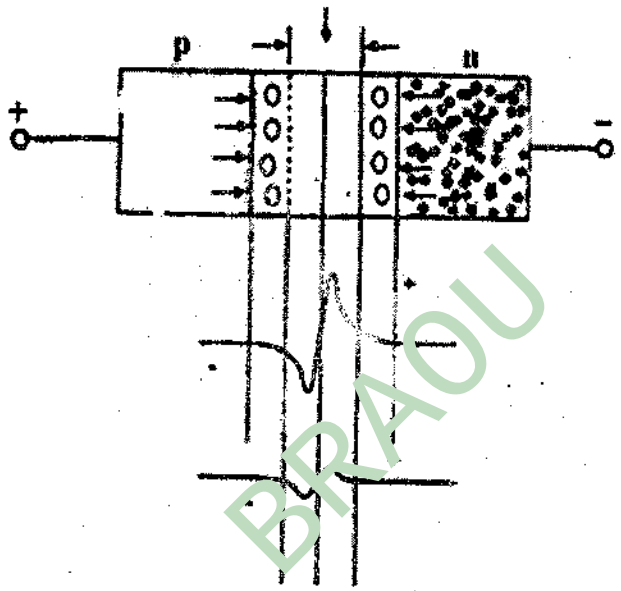


Fig. 2.2(a) forward biasing a pn-junction narrows the depletion region reduces the barrier potential and causes large current flow

DR=Depletion Region; A=Anode; C=Cathode.
V_f=Forward voltage; I_f= forward current; Vr=Reverse voltage; I_r = Reverse current

(b) If we reverse the polarity, of the battery i.e. connect the negative terminal to the p-side and the positive terminal to n-side, a minute current is observed. This current is called the reverse current and the diode is said to be in the reverse biased condition as depicted in Fig. 2.2b.

(a) When the diode is forward biased, the externally applied voltage acts in opposition to the contact potential; thus decreasing the width of the depletion region at the junction. Physically, electrons enter n-side through the cathode lead and as charge carriers in n-side, drift toward the junction. Since the potential barrier at the junction is lowered by the forward bias, electrons cross the junction and the minority charge carriers in the p-side diffuse toward the anode lead. At the same time, holes created at the anode lead by the liberation of bound electrons, drift through the p-side, cross the junction and as minority charge carriers in the n-side, diffuse toward the cathode lead.

In Fig; 2.2(a) the motion of electrons is from left to the right and that of holes is from right to the left. But we should remember that holes and electrons have opposite charges,

hence their motions in opposite directions cause the conventional currents to be added up. The net current flow is in the direction of whole current. In the forward bias condition of diode the resulting high current is due to the motion of majority charge carriers, which by definition are large in number, so that these carriers produce a high current. As a consequence of forward biasing of the diode the depletion region significantly narrows down as illustrated in Fig 2.2(a). The voltage at which the forward current starts is equal to the barrier potential.

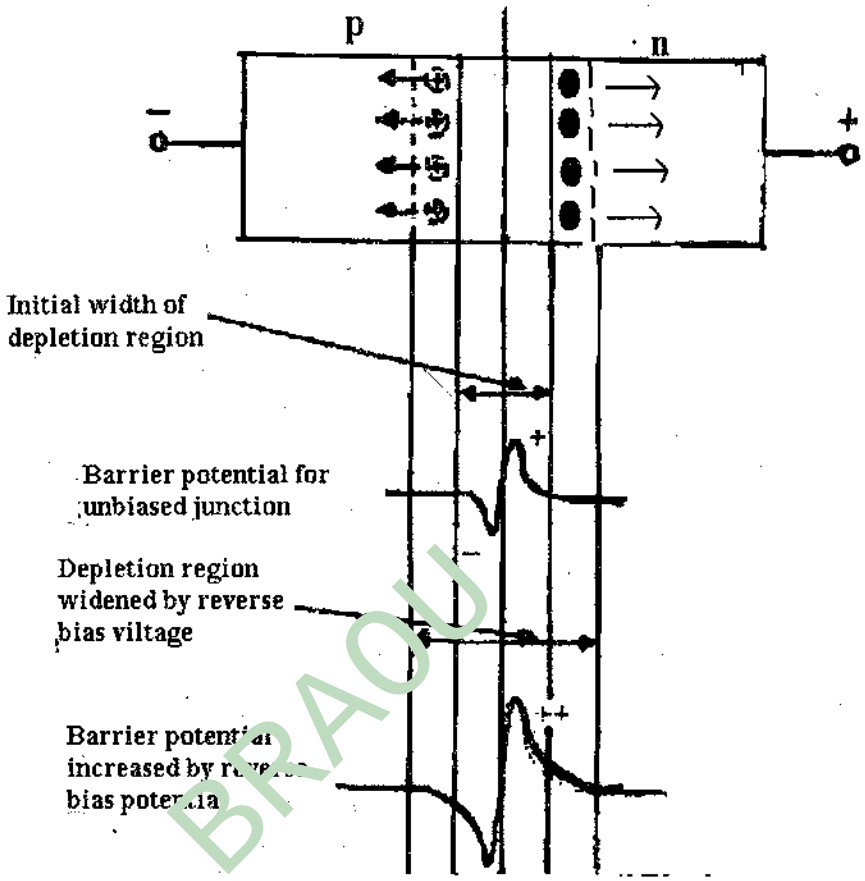


Fig. 2.2(b) pn-junction diode with reverse bias

DR=Depletion Region; A=Anode; C=Cathode.
V_f=Forward voltage; I_f= forward current; Vr=Reverse voltage; I_r = Reverse current

(b) When the diode is reverse biased, the externally applied voltage acts along the same direction as that of contact potential, thus increasing the effective potential barrier across the depletion region. This in turn increases the width of the depletion region (Fig 2.2(b). The external voltage causes the holes in the n-region and electrons in the p-region to move in the direction of the junction. However, these charge carriers are essentially minority charge carriers (small in number) and the resulting current is very low.

The direction of the arrows shown in the figure (a to b) represents the conventional current direction (i.e. positive to negative).

2.4 THE CHARACTERISTICS OF A JUNCTION DIODE

Typical forward characteristics of germanium and silicon diodes are shown in Fig 2.3 Reverse biased characteristics are shown in Fig 2.4

In the forward direction even small Bias voltages result in appreciable currents, while in the reverse direction the current is negligibly small until a certain voltage is reached. It is labeled as V_B on the characteristic curve. This is usually called the breakdown voltage. For voltages more positive than V_B the diode characteristic is given by the following equation called diode equation.

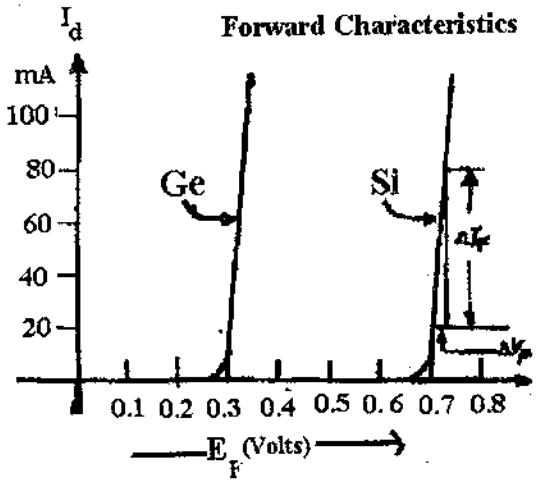
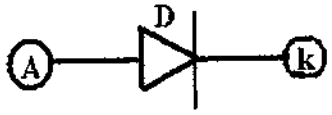
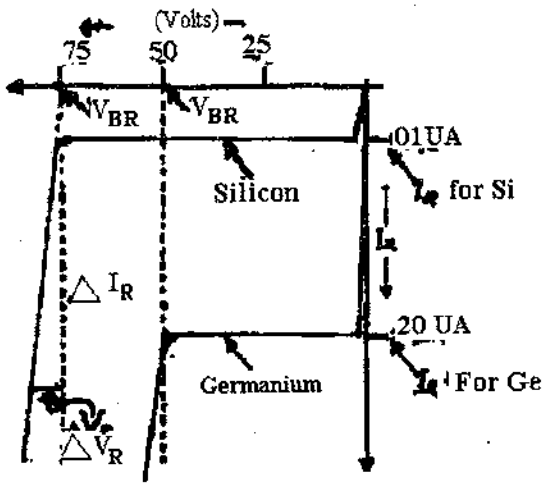


Fig. 2.3Characteristics of Ge and Si diodes under Forward Bias





Reverse Characteristics

Fig. 2.4 Characteristics of Ge and Si diodes under Reverse Bias

$$I=I_0\left[\exp\left(\frac{qV}{kT}\right)-1\right]=I_0\left[\exp(V/\ V_t)-1\right] \qquad \ldots(2.1)$$

q= Electronic Charge

K= Boltzmann Constant $\qquad K=\frac{11600}{n}$ where n= 1or2

$V_t=\frac{kT}{q}=\frac{T}{11,600}$ is the voltage equivalent of temperature 0.026 volts

Where I is the diode current resulting from the externally applied voltage V and I_O is a constant. The magnitude of reverse saturation current is different for different diodes. The factors that govern the value of I_O at room temperature of ≈300K are (a) the type of the material (germanium or silicon), (b) the doping levels of n and p regions. (c) The geometry of the junction etc.

The reverse saturation currents are different for diodes made of germanium and silicon semiconductor materials because of their differences in their energy gaps and mobility of charge carriers. In general; germanium diodes have reverse saturation currents in the microampere range (10^{-6} ampere) while silicon diodes show reverse saturation currents in nanoampere (10^{-9} amperes) range. Temperature plays an important role on the magnitude of the reverse saturation current. As the temperature increases, a large number of covalent bonds are broken down and thus a large number of charge carriers will be

available for conduction. Hence, these devices are temperature sensitive.

In the reverse biased condition as the voltage is increased the diode current saturates quickly. However the voltage cannot be increased in the reverse direction indefinitely. At some critical reverse voltage V_B stated earlier (see Fig. 2.4) large changes in the reverse current for minute changes in the reverse voltage would be observed. The voltage V_B at which this occurs is called the breakdown voltage. There are two mechanisms that can explain the sudden increase in reverse current. The first mechanism is called Zener Breakdown and the second mechanism is called Avalanche Breakdown.

2.4.1 Zener Breakdown

Zener Breakdown occurs when the applied reverse voltage is gradually increased, the electric field set-up across the depletion region becomes large enough to break the covalent bonds. As a result of this breaking of covalent bonds a large number of minority charge carriers are produced far in excess of those, which had set up the reverse saturation current. Due to this sudden increase of large number of minority charge carriers a sudden raise in the reverse current is observed as shown in fig. 2.5.

$$\text{Electronic field strength} = \frac{\text{Reverse Bias Voltage}}{\text{Depletion region width}} \approx 3X10^5\ \text{V/cm} \quad \ldots(2.2)$$

2.4.2 Avalanche Breakdown:

In this mechanism the thermally generated charge carriers collide with the stationary ions in the depletion region. Due to the impact of these fast moving charge carriers there will be breaking of covalent bonds. The collisions result in the liberation of many more mobile charge carriers that are, internally accelerated (due to the presence of the high electric field that exists in the depletion region) in such a way that they now have acquired the capability of producing other free charge carriers upon collision. This cumulative effect is called Avalanche mechanism. As a result the abrupt increase in reverse current takes place with the abrupt creation of many extra charge carriers as explained.

The diodes exhibiting reverse breakdown voltages from about 1 volt to a few hundreds of volts are available commercially. The diodes whose breakdown voltage lies below 5V are usually explained by Zener mechanism and diodes with breakdown voltages above 8 V by the Avalanche mechanism.

2.5 THE POINT CONTACT DIODE.

The point contact diode is a rectifying metal-to-semiconductor junction diode. Several metals may be used including gold, tungsten, molybdenum, chromium, nickel, titanium and aluminum in conjunction with either p-type or n-type silicon. Since the mobility of the electrons is greater than the mobility of holes usually an n-type silicon is often employed as semiconductor since it ensures better high frequency performance. Current flow in these point contact diodes differs from the current flow in conventional pn junction diodes in that minority charge carriers (holes in n type semiconductors) do not take any part in the process. This has the effect of elimination of charge storage effects; enabling switching speeds less than 0.1 nanosecond ($<10^{-9}$ seconds to be achieved. As a consequence of this the point contact diodes can be used at microwave frequencies

The resistance of the zener diode under breakdown condition can be calculated from the graph shown in fig. 2.5 $R_z = \frac{\Delta Vz}{\Delta Iz}$ this is the order of few ohms ..(2.3)

2.6 THE ZENER DIODE

If a pn junction is reverse biased, the majority charge carriers (namely holes in the p region and electrons in the n-region) move away from the junction region (see Section 2.5). The depletion region becomes wider and the absence of charge carrier manifests as a very high resistance region across which the current transfer becomes very difficult. The presence of minority charge carriers and the electron-hole formation in the barrier region account for the presence of a small leakage current. This leakage current remains very low for all reverse voltages up to a certain value. Once this value is exceeded there will be a sudden and substantial rise in the reverse current. The voltage at which the rise in current occurs is called Breakdown Voltage (please see Section 2.3). The breakdown is a reversible process. As described earlier in the mechanisms responsible for the breakdown process are mainly two.

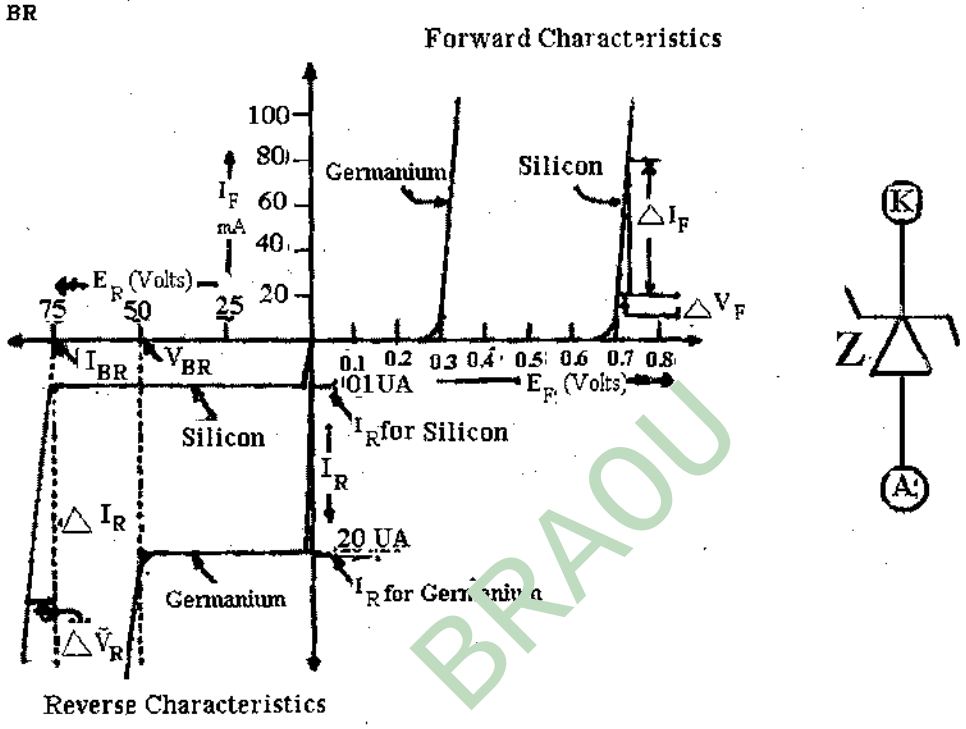


Fig. 2.5 Characteristics of Zener and avalanche breakdown diodes

The first one is Zener breakdown occurs below 8V and the latter is known as Avalanche breakdown, which occurs at higher voltages. Of course nothing precludes the possibility of both the mechanisms being present in the same diode.

Zener diode is a two terminal semiconductor device. It is like the ordinary diode except that it is manufactured to exhibit breakdown in the reverse direction at a specific voltage. These diodes are almost exclusively used as voltage regulators and as reference voltage sources because of their breakdown characteristics. The Zener diode circuit symbol and the typical reverse characteristics of Zener diode with a 6.3V breakdown are shown in Fig. 2.5.

Zener breakdown (6.3 V) is characterised by a 'soft knee' whereas the Avalanche breakdown is abrupt or it is characterised by a 'hard knee' (see Fig. 2.5). Another significant feature of the two types of diodes is their temperature sensitivity. The main difference between these two mechanisms (Zener mechanism and Avalanche mechanism) is that the temperature coefficient of a Zener breakdown is negative while the Avalanche breakdown voltage is positive. The constancy of voltage across the Zener diode makes it useful for many applications.

Zenere diodes are available at present with breakdown voltage ranging 2.2V and 45V and with tolerances between 5% and 20%. The same preferred values for nominal breakdown voltages that are used for resistors. Eg. 2.2V, 4.7V, 6.3V, 15V etc. The range of applications is however very large. They are being used as over voltage protection devices, clippers, limiters, square wave generators etc.

2.7 THE BIPOLAR JUNCTION TRANSISTOR

The bipolar junction transistor (BJT), is a three layer device. It contains two pn junctions as shown in Fig. 2.6. The regions corresponding to the three layers have names suggestive of their functions. The emitter layer emits charge carriers into the base layer where control over the charge carriers can be exercised. These charge carriers are gathered or collected in the collector region eventually. Originally a transistor was made by alloying the emitter and collector regions to a relatively large sample of doped semiconductor material. The sample served as a base for manufacture of transistors and the corresponding region took the name "base" and hence it has been retained even to day.

The base region lies in between the collector and emitter regions. Doping in both the collector and emitter regions with the same type of impurity. (Emitter is doped heavily compared to collector) and the base is always oppositely doped to that of the emitter and collector. Consequently we get two kinds of BJTs. One kind has p-type base and n-type emitter and collector. The other kind has an n-type base and emitter and collector are both p-type. The two types of transistors are termed as npn and pnp respectively.

2.8 CURRENTS IN THE BIPOLAR JUNCTION TRANSISTOR

The two types of transistors (npn and pnp) are shown schematically together with their circuit symbols in Fig. 2.6.

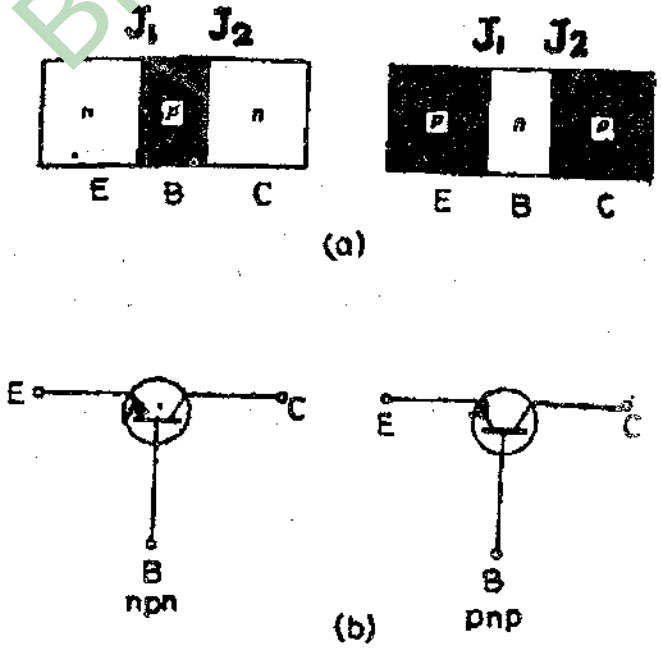


Fig. 2.6 npn and pnp transistors (a) block diagrams (b) circuit symbols

The conventional method and easy way to remember the circuit symbol is to note the direction of the arrow on the emitter terminal. If the arrow "points outwards" it indicates an npn transistor, if the arrow "points inwards" it Indicates a pnp transistor. The direction of the arrow indicates the direction of the conventional current flow in the device.

Now let us see how the BJT works. A fairly large current is caused to flow through the BJT and the control over this current is exercised at the base either by decreasing or increasing the base current. We shall choose an npn transistor as an example first, and similar arguments can be extended to pnp transistors.

In an npn transistor, electrons are the majority charge carriers in the emitter. In order to make these electrons cross the base-emitter junction and enter the base region, an external voltage is applied between the base and emitter terminals. The base and emitter regions constitute a pn junction (diode), which must be forward biased, in order to cause the majority charge carriers (electrons in the n-type emitter) to cross the junction. Once the electrons enter the p-type base, they diffuse through the base. Some of them find their way to the base terminal and flow out and some of them reach collector-base junction. In order to cause these electrons to cross the collector-base junction from the p-type base into the n-type collector a reverse biased voltage should be applied between collector and base terminals. In this manner the electrons that started in the emitter and ended up in the collector constitute the main current, while those electrons that flowed out of the base make up the small controlling current. The schematic representation of various charge carrier emission and current flows for an npn and pnp transistors are shown in fig 2.7(a,b) respectively.

However, we have not considered all the currents in the BJT. As a result of the forward bias on the base-emitter junction, we would expect not only the injection of electrons into the base but also holes to enter from the base to the emitter. We ought to have taken this also into consideration. Although holes from the base region do enter into the emitter region, their effect is negligible on the net emitter current flow in the transistor because the base is very lightly doped where as the emitter is heavily doped. The BJT is purposefully designed in that way. Effectively when the junction is forward biased; the heavily doped n-type emitter produces large number of electrons for conduction, but the lightly doped p-type base has only a small number of holes to offer. Therefore the current across the base-emitter junction in an npn transistor is essentially the result of electron flow.

The reverse bias at the collector-base junction not only transports the electrons from the base into the collector, but also causes another current flow across the collector-base junction. This current is constituted by the minority charge carriers in both, the collector and base regions, namely, electrons from the p-type base and holes from the n-type collector. The current component resulting in this way, from minority charge carriers across the collector base junction is quite small. It is called the collector-base reverse saturation current or collector cut-off current I_{CBO} and as a satuartion current it is very sensitive to temperature.

There is no means of measuring these current components separately inside a transistor. The electrons supplied to the emitter and flowing toward the base correspond to a conventional current flow out of the emitter. Let us designate this current as emitter current I_E, Similarly the electrons flowing out of the base and collector correspond to net terminal currents I_B and Ic respectively. These currents are depicted in Fig. 2.7(a,b) for pnp and npn transistors, together with the internal movement of charge carriers.

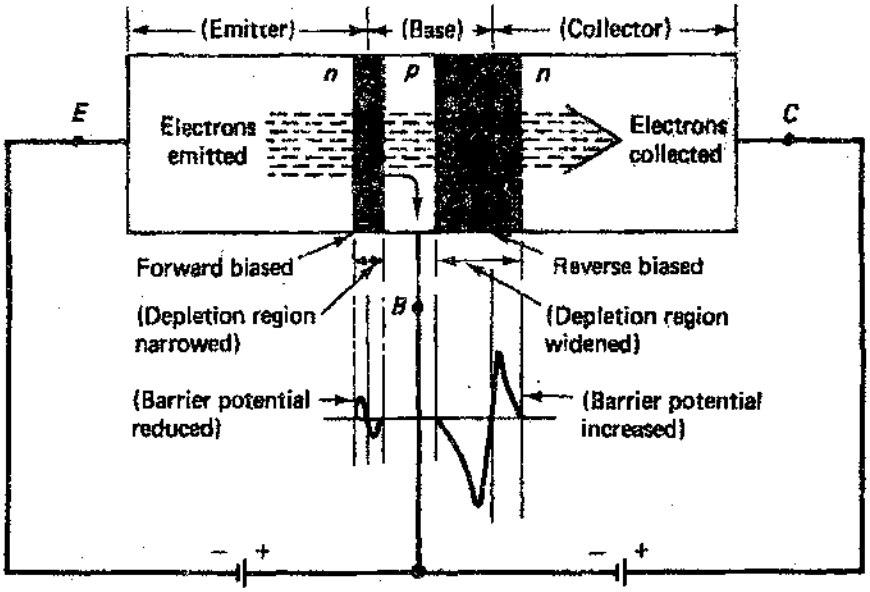
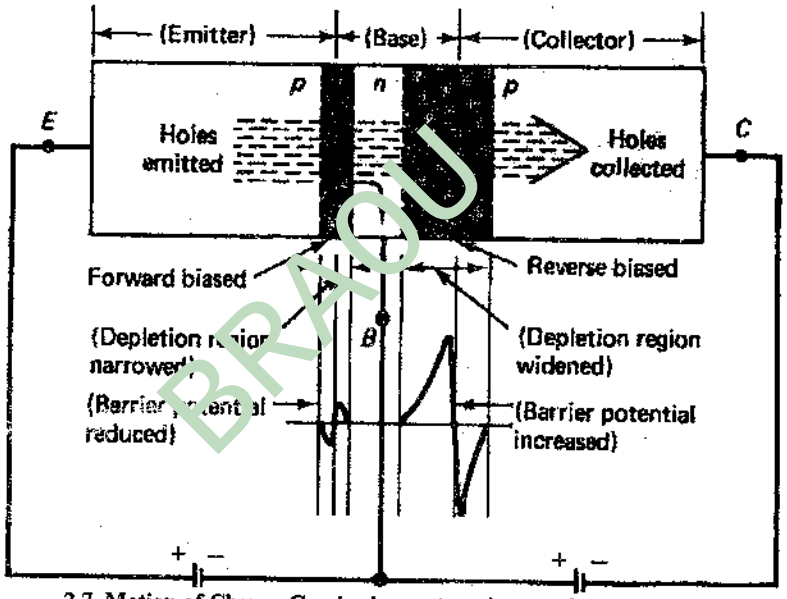


Fig. 2.7(b) Motion of Charge Carriers in a npn transistor and various current components



2.7 Motion of Charge Carrier in pnp transistor and various current components

Fig. 2.7. Movement of charge carriers in an npn transistor. Where E – represents
A. n-type emitter, B. Represents p-type base and, C. Represents n-type collector
B. BEJ = Base-Emitter Junction, CBJ = Collector-base junction

The circuit diagram for the normal operation of an npn transistor with base-emitter diode forward biased and the collector-base diode reverse biased is shown in Fig. 2.8.

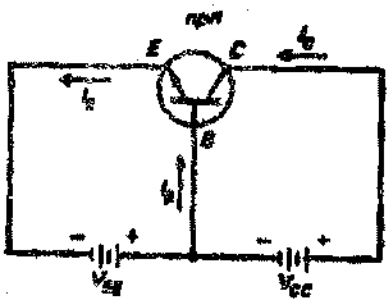


Fig 2.8 Schematic representation of Bias for normal operation of an npn transistor along with the directions of the resulting terminal currents in common base configuration

As a result of the externally applied bias voltages the depletion region at the collector-base junction widens and the depletion region at the base emitter junction narrows down as shown in fig 2.9

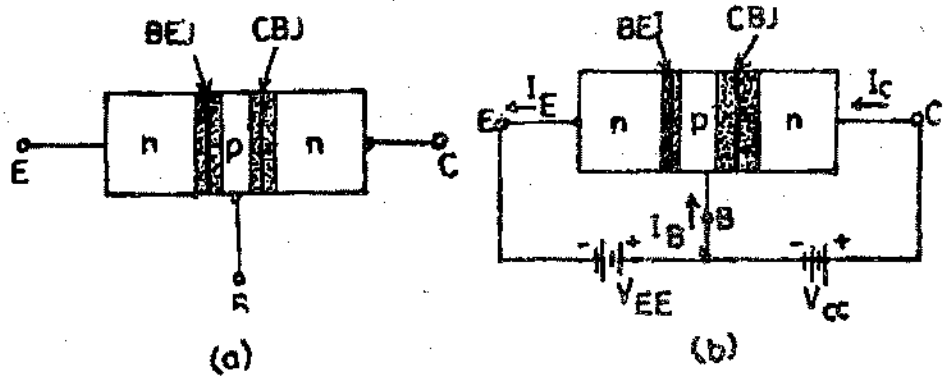


Fig 2.9 Depletion regions inside an npn transistor (a) no bias condition (b) with normal condition BEJ = Base-Emitter Junction; CBJ = Collector-Base Junction

We can see that the net current entering the transistor in Fig. 2.8 is sum of the currents I_C and I_B and the net current leaving the transistor is I_E, Therefore

$$I_E = I_B + I_c \qquad \ldots (2.4)$$

The collector current I_C is made up of the current in the collector resulting from electrons that started in the emitter, tabled I_{nc} together with the reverse saturation current I_{CBO} Thus

$$I_C = I_{nc} + I_{CBO} \qquad \ldots(2.5)$$

The ratio of the electron current in the collector I_{nc} to the total electron current I_E in the emitter, designated α (alpha) is a very important parameter for the bipolar junction transistor where α is defined as

$$\alpha = \frac{I_{nc}}{I_E} \qquad \ldots(2.6)$$

We have already seen that some electrons that started in the emitter are lost in the base, hence I_{nc} is always less than I_E, So α is always less than unity. However it is very close to 1, typically varying between 0.98 and 0.9995. The significance of α is that it is the DC short circuit current gain in the common-base configuration.

If we use the equation (2.5) in defining the equation for α we have

$$\alpha = \frac{I_C - I_{CBO}}{I_E} \qquad \ldots(2.7)$$

Solving for I_C gives an important current relation for the BJT.

$$\alpha\ I_E = I_C - I_{CBO}$$

or

$$I_C = \alpha\ I_E + I_{CBO} \qquad \ldots(2.8)$$

The operation of a pnp transistor is completely analogous to that of npn transistor. The majority charge carriers (here in this case holes) from the p-type emitter are injected into the n-type base by forward biasing the base-emitter junction. Holes are further

transported through the base and some of them are gathered by the collector with the aid of a reverse bias on the collector-base junction. In fact the remaining discussion runs on similar lines as that of npn transistor except with appropriate substutions of p instead of n, n instead of p and hole instead of electron etc have to be in corporated.

There are some aspects common to both npn and pnp transistors. The base-emitter junction is forward biased and the collector-base junction is reverse biased irrespective of the type of the transistors, Equation (2.4) shows that both I_C and I_B are in a direction opposite to that of I_E,

Using Eqns, (2.4) and (2.8) We can write

$$Ic = \alpha\ (I_C + I_B) + I_{CBO} \qquad \ldots(2.9)$$

solving for I_C we get

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO} \qquad \ldots(2.10)$$

We now define another important parameter β (Beta), the DC short circuit current gain in the common-emitter configuration.

$$\beta = \frac{\alpha}{1-\alpha} \qquad \ldots(2.11)$$

Now the equation (2.12) can be written as

$$Ic = \beta\ I_B + (\beta + 1) I_{CBO} \qquad \ldots(2.12)$$

The significance of β, (or h_{fe}) the current gain or current amplification factor is explained in Unit-3 on amplifiers.

2.9 SUMMARY

The diffused charge carriers on either side of pn junction form a region called "Depletion Region". The pn junction allows current in one direction and offers very high resistance in the opposite direction, thus exhibiting the rectifier action.

2.10 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Explain how a depletion layer is formed at the pn junction and discuss the properties of a pn junction.
2. Discuss the biasing arrangement of a pn junction diode and explain its forward and reverse characteristics.
3. Explain the two types of breakdown wizard th eZener and Avalanche breakdown.
4. Explain the functioning of pnp and npn transistors.
5. Define α for a BJT.

6. Deduce the condition $I_c = \beta I_b + (\beta + 1) I_{CBC}$ in a BJT and explain the significance of β.

II Answer the following questions briefly.

1. Explain how a depletion layer informed at the pn junction and the dynamics of the formation of the depletion region.
2. Explain briefly what is the effect of forward and reverse bias on the depletion region in a pn juction diode.
3. Differentiate between the Zener and Avalanche breakdown in a pn junction.
4. What are the, unique characteristics of reverse biased diode.

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UNIT- 3: TRANSISTOR CONFIGURATIONS AND CHARACTERISTICS

Contents:

3.0 AIMS AND OBJECTIVES

This unit explains the various configurations of the transistor Common Emitter (CE), Common Base (CB) and Common Collector (CC) when it is used as an active circuit element. After going through this unit you will be able to workout the different transistor parameters that are useful in electronic circuit design.

3.1 INTRODUCTION

In 1948 Bardeen and Brattain, two American Physicists, announced the invention of the transistor, a new type of device made from semiconducting crystals. Very few at that time could foresee the revolutionary developments that were to follow. These developments are so important and far-reaching as to change the entire outlook of the Science and Technology of electronics. Along with Schokley they could successfully explain the physical principles involved in Transistor Action. In recognition of their work the three Physicists were jointly awarded the Noble Prize in 1956.

3.2 TRANSISTOR BIASING AND CONFIGURATIONS

3.2.1Transistor Biasing Arrangements:

Unit-2 describes the behaviour of the pn junction diode as a rectifying device. Let us now consider two pn junctions J_1 and J_2 as shown in Fig 3.1.

$$I_E=I_B+I_C \qquad \ldots(3.1)$$

Junction J_1 is forward biased so that the majority carriers (in this case, electrons) flow from n-type material to p-type of material. The junction J_2 is reverse biased, so that only a small amount of charge leaks through. This is called the Is leakage current If these two

junctions are connected together and the p-region is made very thin so that the majority charge carriers starting from the emitter do not recombine with holes to any appreciable extent in the base region. Then almost all these majority charge carriers are accelerated towards the collector by the barrier potential across J_2.

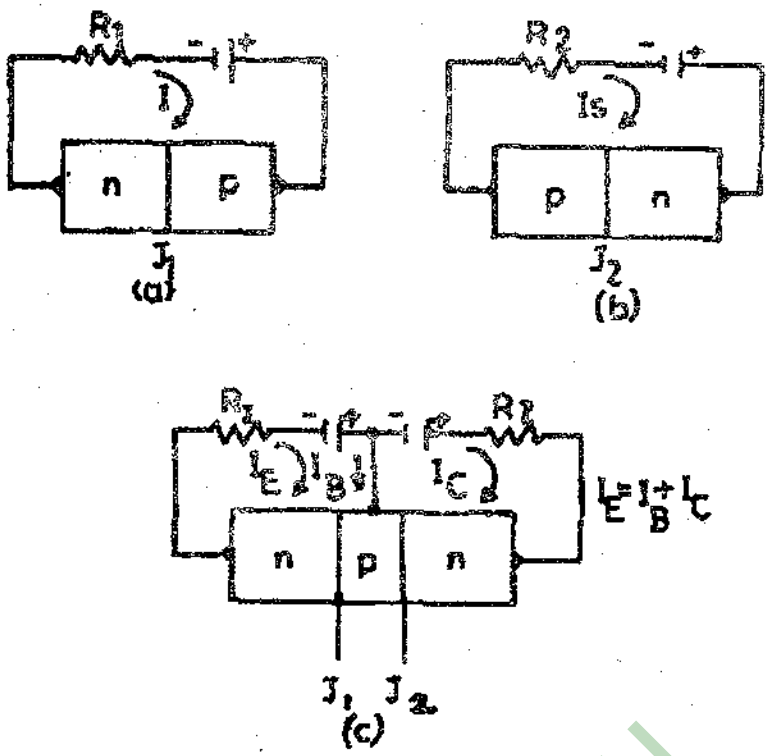


Fig.3.1 Juxtaposition of two pn-junctions (J_1 and J_2) to make a Transistor (a) Junction J_1 is forward biased (b) Junction J_2 is Reverse biased and (c) an npn transistor.

If we call the ratio of current going through J_2 to the current going through J_1 as α (alpha), then

$$I_C = \alpha\ I_E \qquad \ldots (3.2)$$

The holes that recombine with the few electrons in the p-region are supplied by I_B, the base current. Since α is close to unity but less than unity, I_E is almost transferred to the right side of the junction. Because these carriers can be accelerated by the J_2 barrier potential, which can be high, this current can flow through a high external resistance (load resistance) to produce voltage amplification. The three-layer device described here is called the Junction Transistor. The emitter current I_E is equal to the sum of base and collector currents, I_B and I_C. Then

$$I_E = I_B + I_C \qquad \ldots (3.3)$$

When the transistor is connected in an electronic circuit one of the regions (terminals) is connected to the "input" signal, another region (terminal) is connected to the "output" signal line, and the third region (terminal) is connected to a line which is 'common' to both the input and output signals. The circuit configuration is named after the electrode, which is common to both the input and output terminal. Thus we have common-emitter circuits, common base circuits and common-collector circuits. Simple versions of these circuits are shown in Fig. 3.2 a, b, c respectively.

Current gain, Voltage gain are some important parameters of electronic circuits. In this context the word 'gain' simply means the ratio of the amplitudes of the output signal

to the input signal, and does not necessarily have a direct relationship with the efficiency with which it utilizes its power supply.

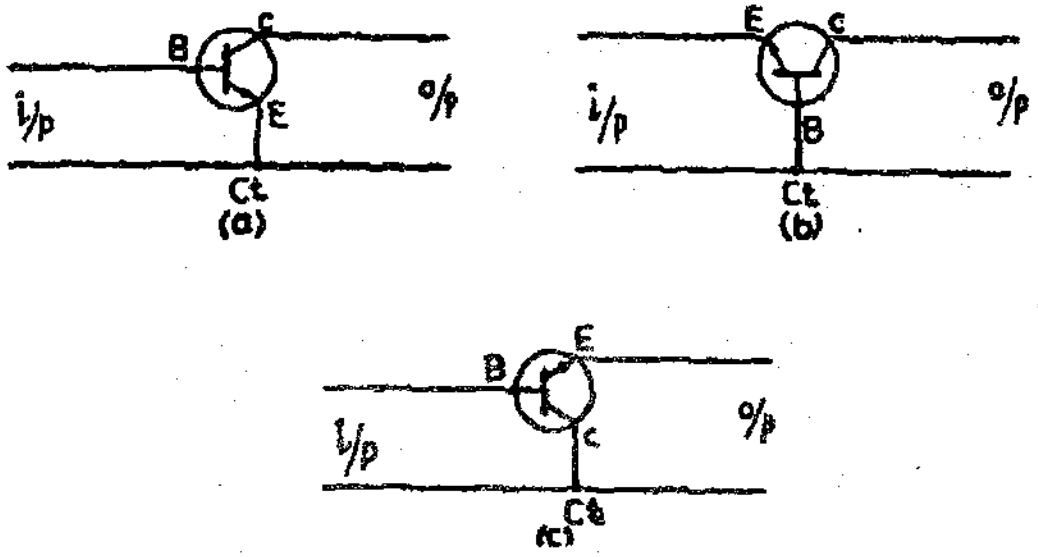


Fig 3.2 npn Transistor Configurations
(a) Commmon-emitter (b) Common base (c) Common Collector
C= Collector; B=Base; E=Emitter; i/p=Input port O/p= Output post
Ct = Common terminal

Other important parameters are the resistances (or impedances) the input impedance between the input terminal and the common terminal and the output impedance between the output terminal and the common terminal. The latter is analogous to the internal resistance of the circuit.

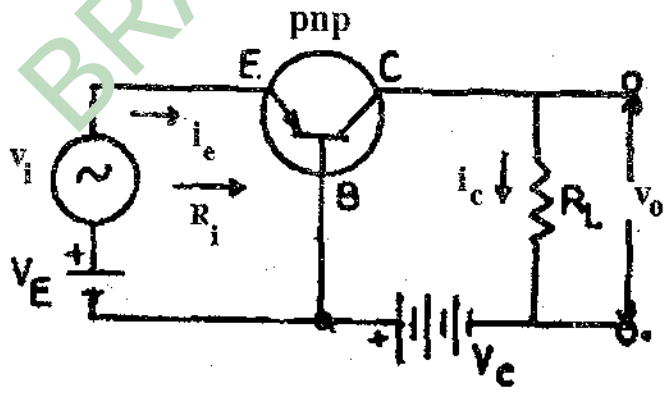


Fig. 3.3 Common-base connection of pnp transistor

The Common Emitter (CE) configuration is the most popular of the three configurations, since it provides high values of current gain; Voltage gain and power gain together with reasonably high value of input impedance. The common-base (CB) configuration gives a high value of voltage gain together with a current gain of unity; its input resistance is low and output resistance is high. The common-collector configuration gives a voltage gain of slightly less than unity together with a high value of current gain; its input resistance is very high and its output resistance is low.

Worked out Example-1: The transistor in the common-base (CB) circuit shown in Fig. 3.3 has a current gain of α. Determine voltage gain, with respect to small signal input variations.

Solution:

The transistor input resistance R_i is related to low forward resistance from emitter to base. The load resistance R_L in the reverse-biased collector circuit can be quite high. Thus

Input voltage = $V_i = i_e R_i$ ...(3.4)

Output voltage = $Vo = I_C R_L$ ...(3.5)

Therefore voltage gain $= \frac{Vo}{Vi} = \frac{I_c R_L}{I_e R_i} = \alpha \frac{R_L}{Ri}$ (from Equ. 3.3)

Where $\frac{I_c}{I_e} = \alpha$ ...(3.6)

While the common-base (CB) circuit offers a current gain, which is nearly unity, it can provide high voltage and power gain. The current gain in CE configuration β may be defined as the ratio of the collector current to the base current.

$$\beta = \frac{I_c}{I_B} \quad ...(3.7)$$

Power gain = current gain x voltage gain

$$A_P = \alpha \text{ X } \alpha \frac{R_L}{R_i} = \alpha^2 \frac{R_L}{R_i} \quad ...(3.8)$$

Example:

Worked out Exarnple-2: Derive the formula for β as a function *of* α

Solution:

We have $I_C = \alpha I_E$ ...(3.9)

$I_E = I_B + I_C$ ...(3.10)

and $\beta = \frac{I_c}{I_B}$ ...(3.1)

α Substituting I_C/α for I_E from Equ. (3.9) and I_C/β for I_B from Equ. 3.11 in Equ 3.10 we obtain

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C \text{ or } \alpha = \frac{\beta}{1+\beta}$$

Simultaneously substituting for $I_B = I_C/\beta$ from Equ. 3.11 and $I_C = \alpha I_E$ from Equ 3.9 in 3.10

$$\beta = \frac{\alpha}{1-\alpha}$$

Worked out Example-3: A transistor has an $\alpha = 0.98$. For an emitter current of 4 ma calculate the base current I_B and also calculate $\beta = I_C/I_B$

Solution:

Collector current α I_E = 0.98 X 4 ma = 3.92 ma. The difference between the emitter and collector current is essentially the base current of 80 μ *A*. Since

$$I_B = I_E - I_C$$

$$\beta = \frac{I_C}{I_B} = \frac{3.92}{0.08} = 49$$

3.3 BIPOLAR TRANSISTOR CHARACTERISTICS:

3.3.1 UNDER COMMON-EMITTER CONFIGURARATION

A circuit to obtain common-emitter static characteristics of an npn transistor is shown in Fig. 3.4.

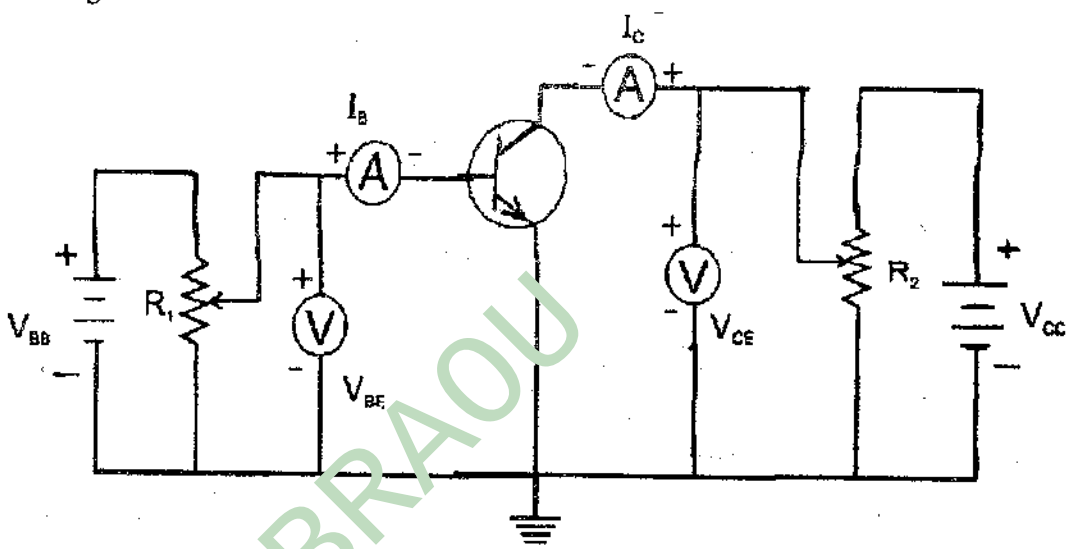
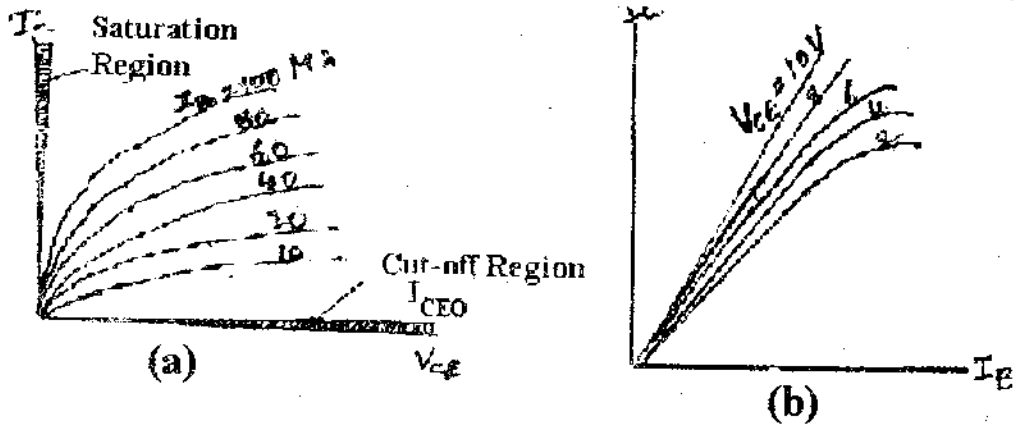


Fig.3.4 Circuit arrangement for the study of characteristics of a transistor in CE Configuration

(i) Characteristic Curves

The characteristics curves are shown in Fig. 3.5 the 500 Ω potentiometers are used in the circuit to vary the base and collector supply voltages.



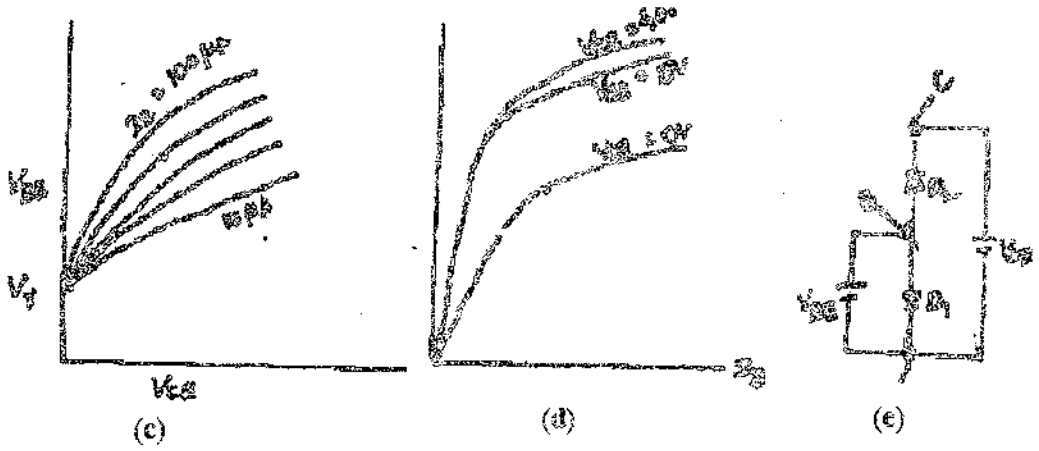


Fig. 3.5. Common-Emitter Characteristics
(a) Output characteristics (b) Forward transfer characteristics (c) A simplified Equivalent circuit of an npn transistor (d) Input characteristics (e) Reverse feedback characteristics CO=Cut - Off region; SR = Saturated region

The output characteristics, Fig. 3.5(a) are particularly useful from a circuit design point of view, since they show how the output current or the collector current I_C varies with the collector-to-emitter voltage V_{CE} over normal working range of voltages. Initially with the base circuit disconnected. The collector current is equal to the intrinsic leakage current in the common emitter mode I_{CEO}. The subscript CE indicates that the current is flowing from collector to emitter and the subscript '0' gives the value of the external base current. In a low power silicon transistor, I_{CEO} has a value of a few tens of nanoamperes. Other values of leakage current of interest in the common-emitter mode are I_{CES} and I_{CEX}.I_{CES} is the collector leakage current with the base short circuited to the emitter and I_{CEX} is the collector leakage current with specified base circuit conditions.

When the collector voltage V_{CE} is held at very low value (ideally Zero) and voltage V_{BE} is applied to the base the transistor is said to be operated in the saturation region. This can be understood with the help of Fig. 3.5c. To a first approximation the transistor may be represented by the Circuit shown in Fig. 3.5c where D_1 is the base-emitter Junction diode and D_2 is the collector-base Junction diode. When V_{BE} is greater than V_{CE} both diodes are forward biased and current flows from the base region to the emitter and collector regions. When this occurs, both diodes are 'saturated' with current carriers hence the name saturation operation.

In electronic logic circuits the transistors are frequently worked in the saturation region of the characteristic. In such circumstances a parameter of some importance is the static value of the saturation resistance. r_{CE} sat. This is the effective resistance between the emitter and collector at some specified point, say A, on the output characteristics. When the collector voltage is greater than the base voltage, the collector Junction becomes reverse biased and the transistor is said to be operating in its unsaturated region. When the transistor is used as a linear amplifier, it is biased to operate in the unsaturated region.

(ii) Hybrid Parameters:

The inter-relationships of V_{CE} I_C V_{BE} and I_{BE} are the transistor characteristics. They are slightly different for each individual transistor and vary greatly from one type of transistor to another. An understanding of these characteristics is essential, as discussed earlier, for determining the relation of the input and output signals in amplifier circuits. They can be determined by using the circuit shown in Fig. 3.4. First I_{DE} is held constant while I_B is measured for various values of V_{CE}. The relationship between I_{CE} and V_{CE} is

then measured for other values of I_B A family of curves is obtained as shown in Fig. 3.5a. These are called output characteristics. If I_B is held constant and the change in V_{BE} is measured as a function of V_{CE}, a family of curves called the reverse feedback or reverse transfer characteristics result they are shown Fig 3.4e. If V_{CE} is held constant, and V_{DE} is measured as a function of I_{BE} a family of input characteristics (Fig. 3.5 d) results.

The slopes of the curves yield corresponding transistor parameters as designated below and they are given a special nomenclature because of their importance. These parameters are called hybrid parameters or h-parameters since both impedances and conductance's are considered in the analysis.

$\frac{\Delta I_C}{\Delta V_{CE}} \Big/ I_B$=Const = h_{α} = output admittance (mhos)

$\frac{\Delta I_C}{\Delta V_{CE}} \Big/ I_B$=Const = h_{re} reverse voltage ratio (a numeric)

$\frac{\Delta I_C}{\Delta I_B} \Big/ V_{CE}$=Const = h_{fe} =forward current gain (a numeric)

$\frac{\Delta V_{BE}}{\Delta I_B} \Big/ V_{CE}$ =Const = h_{ie} = input impedance (ohms)

For a typical transistor the h-parameters under CE configuration are

h_{ie} =2.2 KΩ h_{oe} 33mhos or $1/h_o$ = 33 KΩ

h_{fe} = 250 h_{re} = 2.5×10^{-4}

An observation of the above characteristics indicates that the input impedance h_{ie} moderately high, current gain h_{fe} is very high, output impedance $1/h_{oe}$ is also high. This configuration gives the highest current gain, voltage gain and power gain.

3.3.2 Under Common-Base Configuration Combined Characteristics

The circuit arrangement for obtaining common base static characteristics the is shown in fig.3.6

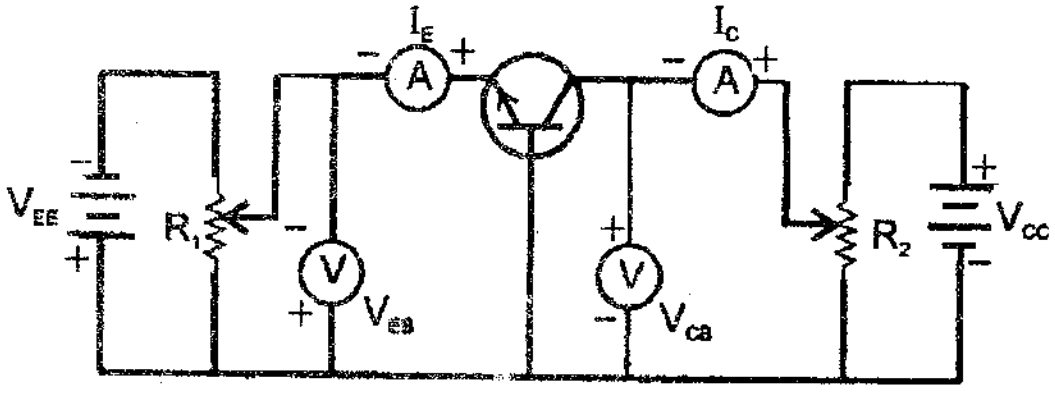


Fig3.6 Circuit arrangement for the study of charecterstics of atrnsistor in CB configuration

$\frac{\Delta I_C}{\Delta V_{BC}}$ / I_E = Const = H_{ob} =output admittance

$\frac{\Delta I_C}{\Delta I_B}$ / V_{BC} =Const = h_{fb} =forward current gain or transfer ratio

$\frac{\Delta V_{BE}}{\Delta V_{BC}}$ / I_E = Const = h_{rb} reverse voltage transfer ratio or reverse feedback ratio

The ratio $\frac{\Delta I_C}{\Delta I_B}$ is known as the static value of the *forward current ratio.* For convenience, in transistor circuit analysis, all currents are assumed to flow into the transistor and paradoxically in this case, as will be seen from the following this leads to h_{FB} having a negative value. In Fig. 3.6a, it can be seen that both I_{CB} and I_{EB} appear to enter into the transistor, but a moment's notice will show that, in fact, one of the two currents must flow out of the transistor. Thus if a collector current of 98 mA flows into transistor and the base current is 2 mA then an emitter current of 100 mA flows out of the transistor. Hence

$$h_{FB} = \frac{+98}{-100} = -0.98$$

The value of h_{FB} usually lies between -0.98 and -0.998. The small-signal common base current gain α is the magnitude of the ratio I_C/I_E without regard to the sign, and

$$\alpha = -h_{FB}$$

The leakage current of the transistor in common-base mode is the collector-to-base current with the emitter (input) open circuited. This leakage current is designated as I_{CBO} the relationship between two values of leakage current is given by

$$I_{CBO} = I_{CEO} \quad (1 + h_{FB})$$

For a typical transistor the h-parameters under CB configuration are

$h_{iB} = 0.95 \cdot$ $\quad h_{OB} = 0.49$mhos or $1/h_{OB} = 2M\Omega$

$h_{rB} = 0.2 \times 10^{-4}$

An observation of the above characteristics indicates that input impedance h_{iB} is very small, current gain $h_{fB} \approx 0.98$ and output impedance $1/h_{OB}$ $2M\Omega$ very high. Hence, it offers high voltage gain and high current gain.

3.3.2 The Common-Collector Configuration Mixed Characteristics

(i) Characteristics

The circuit arrangement for obtaining common static collector characteristics is shown in fig 3.8

First V_{CE} is kept constant. Then I_B is varied ad the corresponding V_{BE} variation is recorded. Then the experiment is repeated for various values of I_B and a set of curves known as *Input Characteristics* is obtained as shown in Fig 3.9(a)

If I_B is kept constant. Then V_{CE} is varied and the corresponding I_E variation is recorded. Then the experiment is repeated for various values of I_B and a set of curves known as the *Output Characteristics* obtained as shown in Fig. 3.9(b)

(i) Characteristics

First V_{BC} is kept constant. Then I_E is varied ad the corresponding V_{BE} variation is recorded. Then the experiment is repeated for various values of I_E and a set of curves known as *Input Characteristics* is obtained as shown in Fig. 3.7(a)

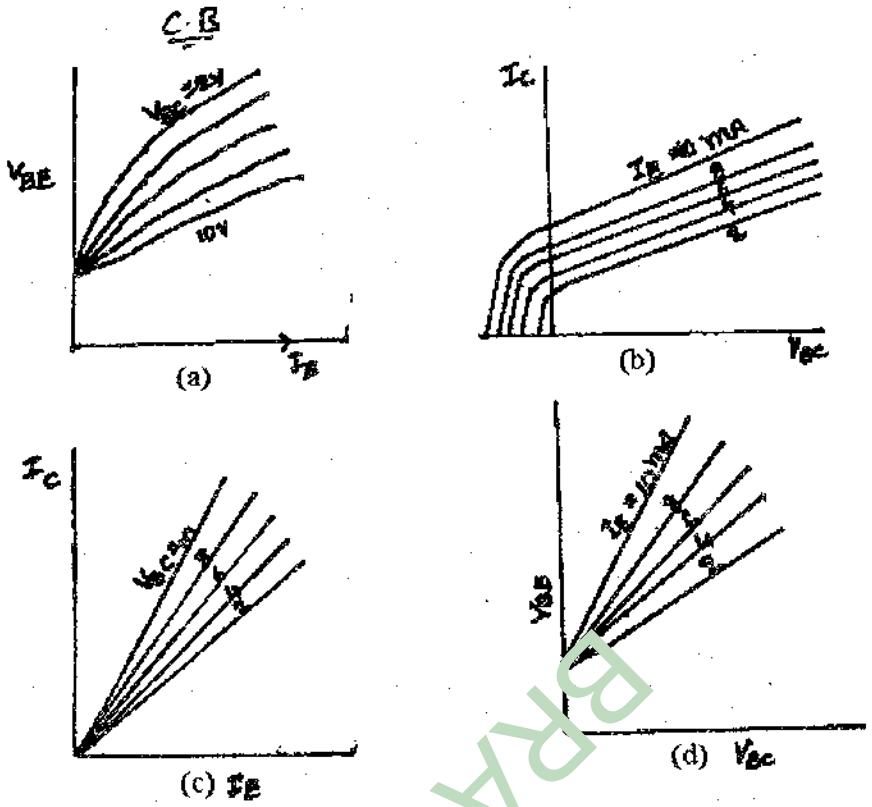


Fig 3.7 Common Base Characteristics
(a) Input Characteristics (b) Output Characteristics (c) forward Transfer Characteristics
(d) Reverse Feedback Characteristics

If I_E is kept constant. Then V_{BC} is varied and the corresponding I_C variation is recorded. Then the experiment is repeated for various values of I_E and a set of curves known as the *Output Characteristics* is obtained as shown in Fig3.7 (b)

If V_{BC} is kept constant. Then the variation of I_C for different values I_E is recorded. Then the experiment is repeated for various values of V_{BC} and a set of curves known as the *forward current transfer characteristics* is obtained as shown in Fig3.7 (c)

If on the other hand, I_E is kept constant and the variation of V_{BE} with V_{BC} is recorded. Then the experiment is repeated for different values of I_E and a set curves known as *reverse transfer characteristics* is obtained as shown in Fig. 3.7 (d)

The slopes of these sets of characteristics yield different hybrid parameters as

(ii) Hybrid Parameters

$$\frac{\Delta V_{BE}}{\Delta I_E} \Big/ V_{BC} = h_{ib} = \text{Input impedance}$$

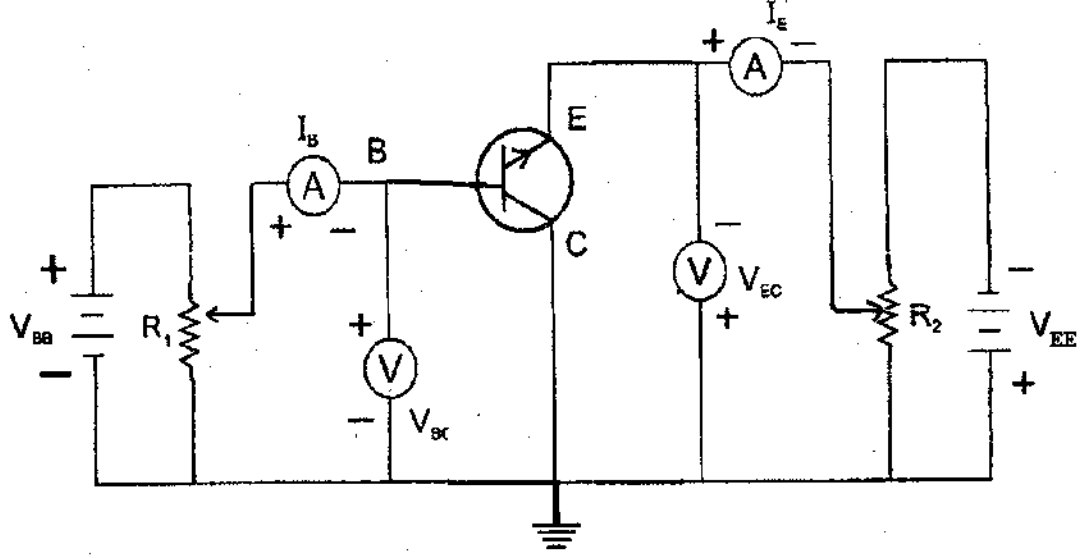


Fig 3.8 Circuit arrangement for the study of transistor in Common Collector Configuration

If V_{CE} is kept constant. Then the variation of I_E for different values I_E is recorded. Then the experiment is repeated for various values of V_{CE} and a set of curves known as the *forward current transfer characteristics* is obtained as shown in Fig 3.9(c)

If on the other hand, I_E is kept constant and the variation of V_{BC} with V_{CE} is recorded. Then the experiment is repeated for different values of I_E and set curves known as *reverse feedback characteristics* is obtained as shown in Fig. 3.9. (d)

An observation of the characteristics shown that the input impedance h_{ic} = 220KΩ and the output impedance $1/h_{oc}$ 1.6 KΩ. Hence, this configuration offers highest input impedance and lowest output impedance highest current gain. Hence, it Is used as isolation amplifier.

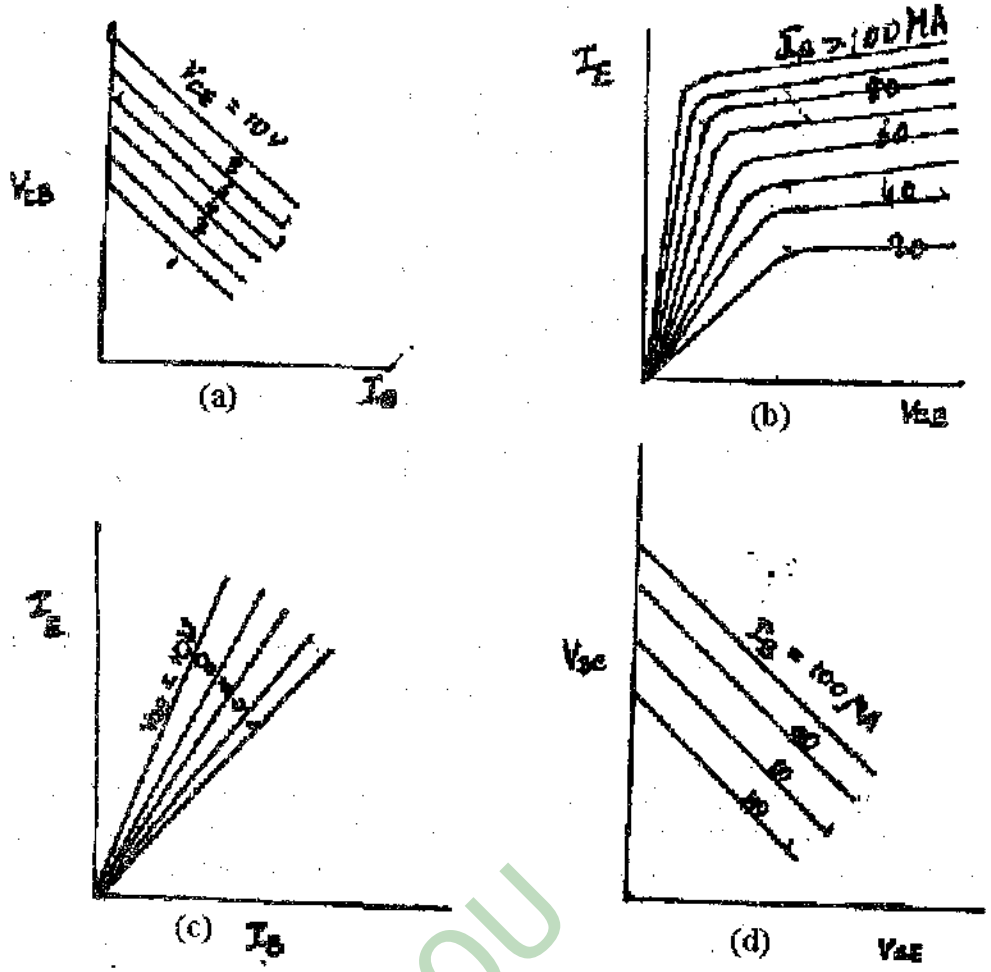


Fig. 3.9. Common-Collector Configuration
(a) Input and (b) Output characteristics at low base current of the 2N 929 transistor behaviour of the common collector configuration (CC).

(ii) Hybrid Parameters

The slopes of these sets of characteristics yield different hybrid parameters as

$\frac{\Delta V_{BC}}{\Delta I_B} \Big/ V_{CE} = h_{ic}$ = Input impedance

$\frac{\Delta I_E}{\Delta V_{CE}} \Big/ I_B$ = Const = H_{oc} =output admittance

$\frac{\Delta I_E}{\Delta I_B} \Big/ V_{CE}$ =Const = h_{fc} =forward current gain or transfer ratio

$\frac{\Delta V_{BC}}{\Delta V_{CE}} \Big/ I_E$ = Const = h_{rc} = reverse voltage transfer ratio or reverse feedback ratio

Transistors are frequently used in this configuration as buffer stages between circuits widely differing in impedances but common collector parameters are rarely quoted in manufacturer's literature. Fig. 3.9 shows the family of curves particularly descriptive of the behaviour of the common collector configuration

Worked Example-4: For a common-collector configuration using the 2N929 transistor,

V_{CE}=5V and I_B=0.6 mA. Find the collector current I_C and the base-emitter voltage drop V_{BE}.

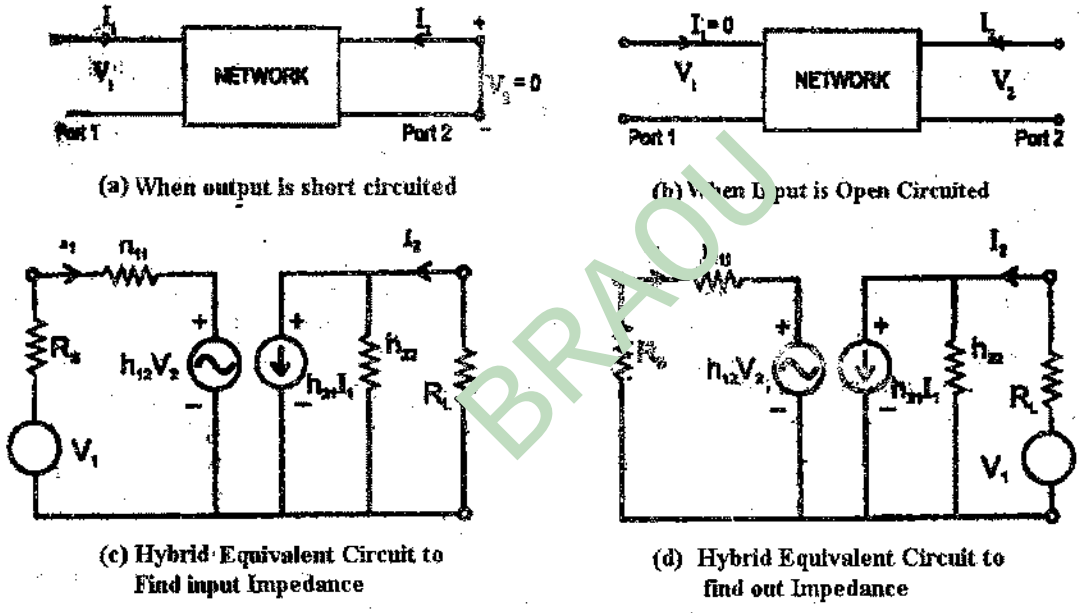
Solution:

Using the common-collector characteristic curves of Fig. 3.8. In Fig 3.7, operating point P is located. By interpolation, $I_B = 4.5\ \mu A$ (between the 18 = 0 and 18 = *4 μ A).* IC = 0.6 mA, in Fig 3.8, the point P is located corresponding to $I_B = 4.5\ \mu A$ and V_{CE} > IV. The base-emitter voltage drop is found to be V_BE = 0.53 V.

3.4 THE HYBRID EQUIVALENT CIRCUITS OF TRANSISTOR

(a) General Two-Port Network or Hybrid Equivalent Circuit

The hybrid equivalent is the most widely used for describing the characteristics of the transistor. It is termed hybrid because it combines both admittance and impedance parameters known as the h-parameters.



(a) When output is short circuited

(b) When Input is Open Circuited

(c) Hybrid Equivalent Circuit to Find input Impedance

(d) Hybrid Equivalent Circuit to find out Impedance

Fig. 3.10. Transistor as a two-port network 1 = Input. 2 = Output;

The ease of measurement of the h-parameters has contributed to its widespread adaptation. Two types of hybrid parameters are usually quoted for transistors, namely, small-signal h-parameters and large-signal h-parameters.

Small sign parameters are used in cases where the magnitude of the input signal is small (the input signal is very much less than the DC power supply voltage used). Large-signal parameters generally employed where the input signal is comparable to dc voltages, as occurring in the case of switching circuits, or logic circuits and power amplifiers. The small signal model is usually specified by either the open-circuit Z-parameters or the short-circuit Y-parameters or h-parameter. As discussed earlier, the h-parameters are widely used as they can be measured easily. In addition, they provide quick estimates of typical operating conditions. The four h-parameters can be defined with the help of two-port network shown in Fig. 3.8.

The two-port network can be represented as follows. In this case the input current I_1 and the output voltage V_2 are taken as independent variables. The input voltage and output current can be written using 'h' parameter as follows

$$V_1 = h_{11} I_1 + h_{12} V_2 \quad \ldots(3.12)$$
$$I_2 = h_{21} I_1 + h_{22} V_2 \quad \ldots(3.13)$$

Also in matrix representation

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad \ldots(3.14)$$

When h_{11}, h_{22} are determined by making output of the two-port network is short-circuited. h_{12} and h_{22} are determined by making input of the two part network is open circuited.

When output is short circuit i.e., $V_2 = 0$

Hence from Equ. 3.6 $h_{11} = h_i = \left.\frac{V_1}{I_1}\right|_{when\ V_2=0} = Input\ \ Inpedence$

From Equ. 3.7 $h_{21} = h_f = \left.\frac{I_2}{I_1}\right|_{when\ V_2=0} = forward$ current gain

When the Input is open circuited,

From Equ.3.6 $h_{21} = h_f = \left.\frac{V_1}{V_2}\right|_{when\ I_2=0} = reverse\ Voltage$ gain.

From Equ.3.7 $h_{22} = h_O = \left.\frac{I_2}{V_2}\right|_{when\ I_1=0} = output\ impedence$

The analysis of two-port network can be adopted for the small signal transistor amplifier circuits also and the corresponding hybrid parameter can be evaluated for different configurations. Hence,

$$V_i = h_i I_O + h_r V_O \quad \ldots(3.15)$$
$$i_O = h_f I_i + h_O V_O \quad \ldots(3.16)$$

Where V_i is the (rms voltage) signal applied to the input of the transistor, i_i is the rms input current; V_O is the rms value of the small-signal output voltage and i_O is the rms value of the output current. The subscripts i,f,o and r stand for input, forward, output, and reverse respectively.

Depending on the circuit configuration, i.e., common-emitter (CE), common-base (CB), common-collector (CC), other subscripts are given to the parameters namely,

e,= cemmon-emitter configuration

b = common-base configuration

c = common-collector configuration respectively.

Thus the equations (3.4) and (3.5) for common emitter configuration take the form

$$V_{be} = h_{ie} I_{be} + h_{re} V_{ce} \quad \ldots(3.17)$$
$$i_e = h_{fe} I_{be} + h_{oe} V_{ce} \quad \ldots(3.18)$$

where

h_{ie} = input impedance (in ohms)
h_{oe} = output admittance (in mhos)

h_{fe} = forward .current ratio (no units)
h_{re} = reverse voltage ratio (no units)

In a similar manner, the parameters in CB configuration are h_{ib}, h_{ob}, h_{fb} and h_{rb}' In the CC configuration, we have, h_{ic}, h_{oc}, h_{fc} and h_{rc}. To be strictly accurate, h_{ie} and h_{fe} should both be measured with V_{ce} = 0, i.e., output should be short circuited to ac signals. Similarly h_{re} and h_{oe} should be determined with i_{be} = 0, i.e., the input should be open circuited to signal frequencies. The h-parameters are in general different for each configuration. However one set of parameters can be converted into another set with the help of the relations listed in Table 3.1.

TABLE 3.1 Conversion of h-parameters

common-emitter	Common-collector	Common-base
h_{ie}	$\frac{h_{ob}}{1+h_{fo}}$	h_{ic}
h_{re}	$\frac{h_{ob}h_{ib}}{1+h_{fo}}$ - h_{rb}	1 - h_{rc}
h_{fe}	$\frac{-h_{fb}}{1+h_{fb}}$ - h_{fb}	-(1+h_{fc})
h_{oe}	$\frac{h_{ob}}{1+h_{fb}}$	h_{oc}

The equivalent circuit satisfying general h-parameter Eqn (3.4) and (3.5) is shown in Fig. 3.9(a) and that for common emitter configuration. Common base and common collect configurations are show in Fig.3.9(b,c,d) respectively.

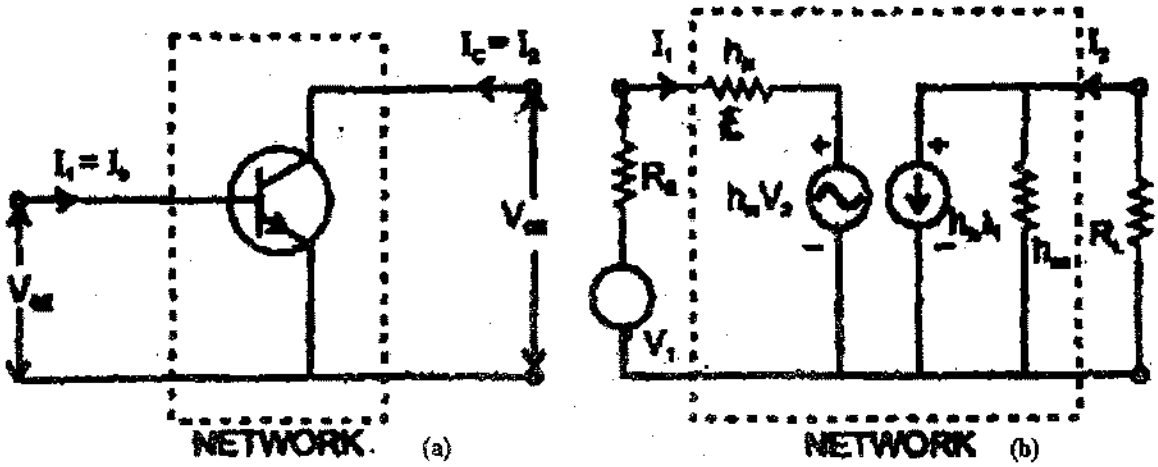


Fig 3.11 CE Amplifier and Its Hybrid Equuivalent Circut

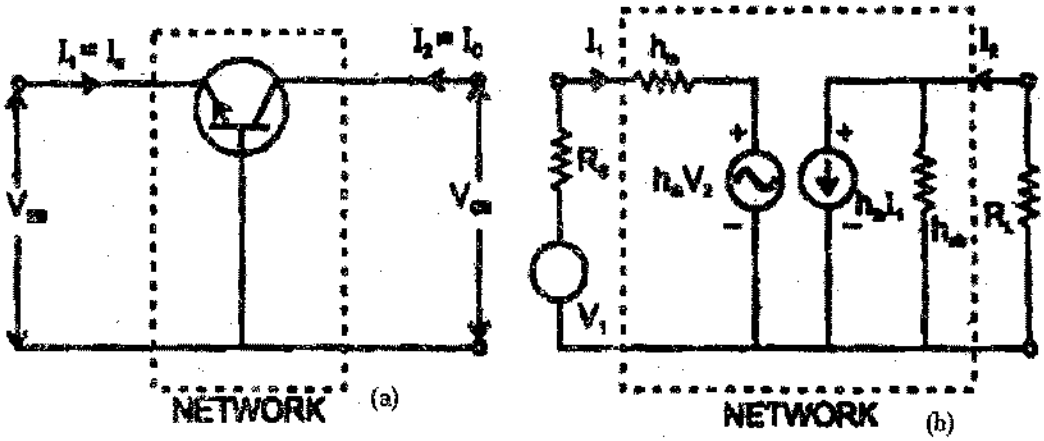


Fig 3.12 CB Amplifier and its Hybrid Equialent Circuit

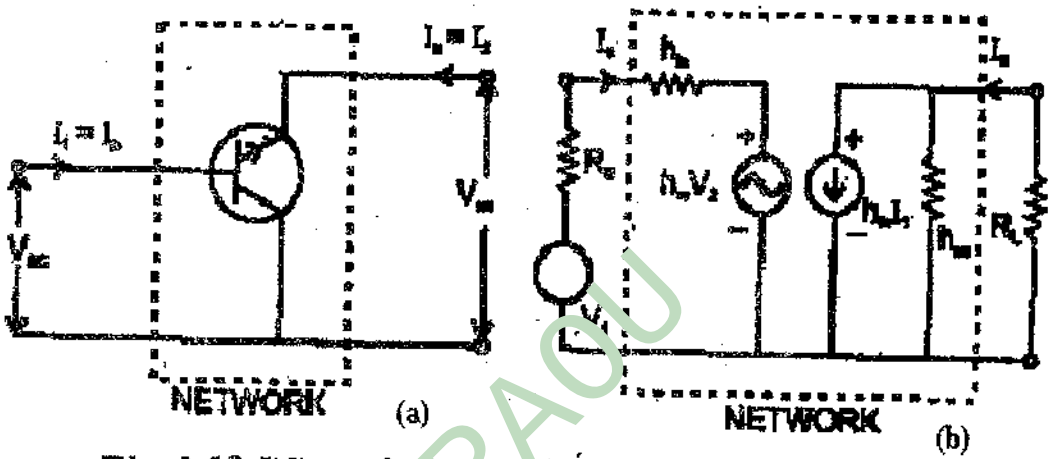


Fig. 3.13 CC amplifier and its Hybrid Equalent Circuit

equations (3.6) and (3.7) is shown in Fig. 3.9(b). Typical h-parameter values for the transistor 2N 929 (pnp transistor) in all the three configurations are given in Table 3.2.

TABLE 3.2-Typical hybrid parameters of2N929 transistor

h-parameter	CE	CB	CC
h_I	2200 Ω	7.5 Ω	220 KΩ
h_R	$2.5x10^{-4}$	$0.268 X 10^{-4}$	Ω 1
h_f	290	-0.996	-291
h_O	30 μ mhos	0.49 μ mhos	600 μ mhos
$r_O = 1 / h_O$	33KΩ	2MΩ	1.6KΩ

Worked Example-5: Making use of the data presented in Table 3.1 draw the hybrid equivalent for common-emitter configuration.

Solution:

$h_{oe} = 30 \times 10^{-6}$ mhos

$h_{fe} = 290$

$h_{ie} = 2200\ \Omega$

$h_{re} = 2.5 \times 10^{-4}$, for $V_{CE} > 1$

neglecting $h_{re} V_{CE}$ the equivalent circuit

Equivalent circuit corresponding to the h-parameters is given above

3.5 SUMMARY

Collector, base and emitter are the three terminals of a transistor. Among the three configurations of a transistor circuit common emitter configuration is more useful. The hybrid parameters describe the characteristics of a transistor.

3.6 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Give brief survey of the three-transistor configuration and explain in detail the significance of common emitter configuration.
2. Write a note on h-parameters of a transistor.
3. Explain which of the three configurations provided the maximum voltage gain power gain.
4. Which of the configurations offers the maximum input impedance and minimum impedance.

3.7 REFERENCES

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2. Integrated Electronics – Analog and Digital Circuits — Jacob Millman and C.C. Halkias
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UNIT 4: SPECIAL SEMICONDUCTOR DEVICES

Content

4.0 AIMS AND OBJECTIVES

The aim of this unit is to familiarise you to the principles and working of the four special semiconductor devices namely Tunnel diode, Uni-junction Transistor, Field effect transistor and silicon controlled rectifier.

After going through this unit you will be able to explain the simple and important applications of the four special semiconductor devices.

4.1 INTRODUCTION

With the advent of semiconductor technology, numerous devices have appeared on the market. A study of the working of these devices is essential for understanding the behaviour of different circuits. This unit deals with the principles of working of four important semiconductor devices. The choice of these four devices has been dictated by the demands of present day technology.

4.2 THE FIELD EFFECT TRANSISTOR

Field effect transistors (FET) are voltage-operated devices. Unlike bipolar transistors, FET's require virtually no input current, and this gives them an extremely high input resistance. There are two major categories of field effect transistors, junction FET's (JFET's) and insulated gate FET's (IGFET's). These are further subdivided into p-channel and n-channel devices.

The operating principle of the n-channel junction field effect transistor (JFET) is illustrated by the block representation in Fig. 4.1. A piece of the n-type material, referred to as the channel, has two smaller pieces of p-type attached to its sides, forming pn-junctions. The channel's ends are designated the drain and the source, and the two pieces of p-type material are connected together and their terminal is called the gate. With the gate terminal not connected, and a potential applied (positive at the drain, negative at the source), a drain current (I_D) flows as shown in Fig. 4.1(a) When the gate is biased negative with respect to the source [Fig. 4.1(b)], the pn-junctions are reverse biased and depletion regions are formed. Since, the channel is more lightly doped than the p-type gate blocks, the depletion regions penetrate deeper into the channel. Since a depletion region is a region depleted of all charge carriers, it behaves as an insulator. The result is that the channel is narrowed, its resistance is increased, and I_D is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center

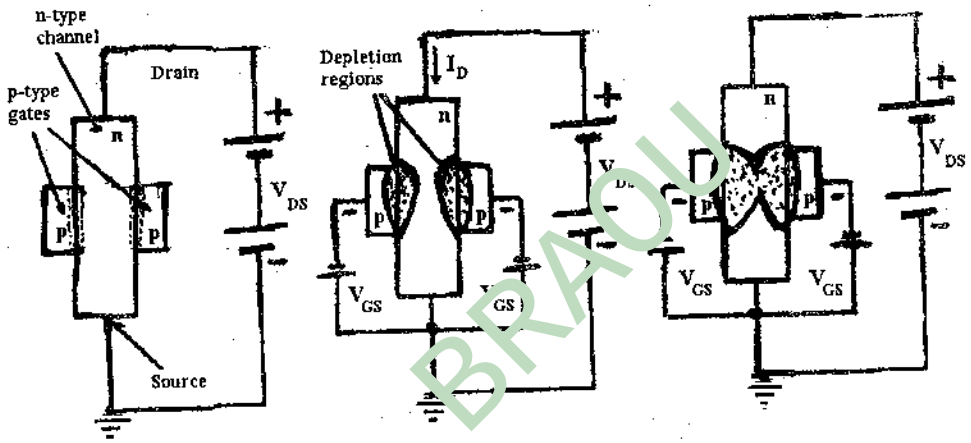


Fig. 4.1(c), and I_D is cut off completely.

(a) No Bias Voltage Negative gate On Gates

(b) Small Negative Gate Source Bias

(c) Large Source Bias

Figure 4.1 Principle of the n-channel JFET.

When a signal is applied to the gate, the reverse voltage on the junctions is increases as the signal voltage goes negative and decreases as it goes positive. Consequently, as the signal goes negative the depletion regions are widened, the channel resistance is increased, and the drain current is reduced. Also, as the signal goes positive the depletion regions recede, the channel resistance is reduced, and the drain current is increased.

The name field effect device comes from the fact that the depletion regions in the channel are the result of the electric field at the reverse-biased gate—channel junctions.

The term Uni-Polar transistor is sometimes applied to FET, because unlike a bipolar transistor the drain current consists of only one type of charge carriers, electrons in the n-channel FET and holes in the p-channel device.

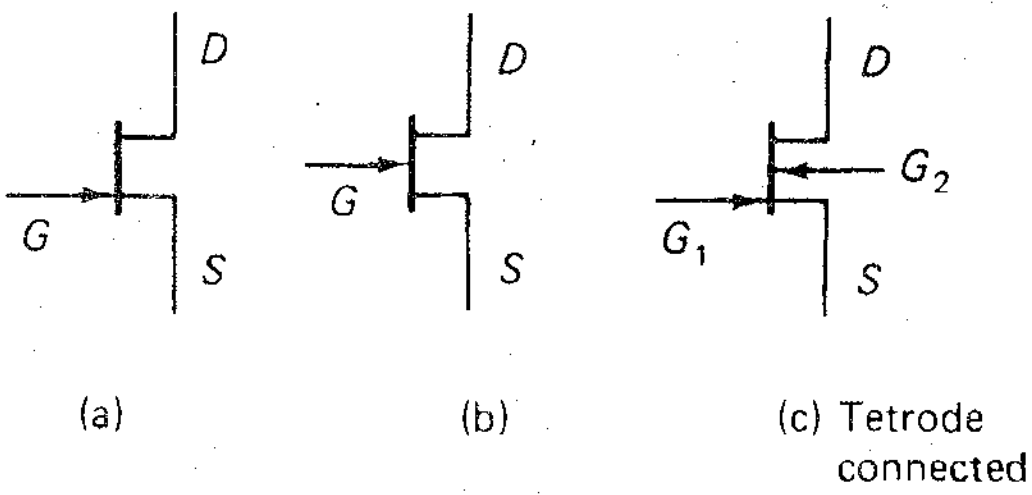


Figure 4-2. Circuit symbols for the n-channel IFET

The symbol for the n-channel JFET is shown in Fig.4.2 As for the convention the arrowhead always points from p to n. For an n-channel device, the arrowhead points from the p-type gate toward the n-type channel

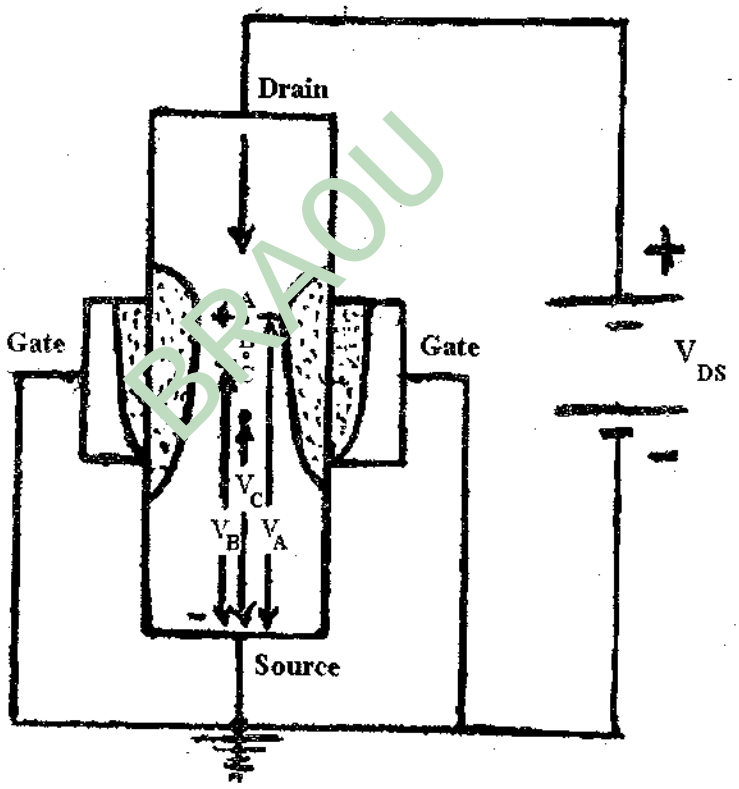


Fig. 4.3 Internal voltage drops along the channel and the resulting depletion regions.

An n-channel JFET is shown in Fig. 4. 3with the gate connected directly to the source terminal. When a drain voltage (V_D) is applied, a drain current I_D flows in the direction shown.

Since the n-material is resistive, the drain current causes a voltage drop along the channel. In the portion of the channel between gate and source I_D causes a voltage drop, which biases the gate with respect to that part of the channel close to the gate. Thus, in Fig. 4.3, the gate regions are negative with respect to point A by a voltage V_A. This will cause the depletion regions to penetrate deeper into the channel at point A by an amount proportional to V_A. Between point B and the source terminal the voltage drop along the channel is V, which is less than V_A. Therefore, at point B the gate is at V_B with respect to the channel, and the depletion region penetration is less than at point A. From point C to

the source terminal, the voltage drop V_C is less than V_B. Thus, the gate channel junction reverse bias (at point C) is V_C volts, and penetration by the depletion regions is less than at A or B. This difference in voltage drops along the channel, and the consequent variation in bias, account for the shape of the depletion regions penetrating the n-channel. That is the deflection region extend deeper into the channel from source end to the drain end or decreases from drain end to source end.

When the gate is connected directly to the source (i.e., no external bias), V~ =0. The characteristic for V_{GS} = 0 is plotted in Fig. 4.4. When V_{DS} = I_D =0, and the voltage between the gate and all points in the channel is also equal to zero. When V_{DS} is increased by a small amount, a small drain current flows, causing some voltage drop along the length of the channel. This reverse biases the gate channel junctions by a small amount, causing little depletion region penetration, and having negligible effect on the channel resistance. With further small increases in V_{DS} the drain current increase is nearly linear, and the channel behaves as a resistance of almost constant value. The region of the characteristic between V_{DS} =0 and V_{DS} = V_P is termed the channel "ohmic region," because the channel is behaving as a resistance.

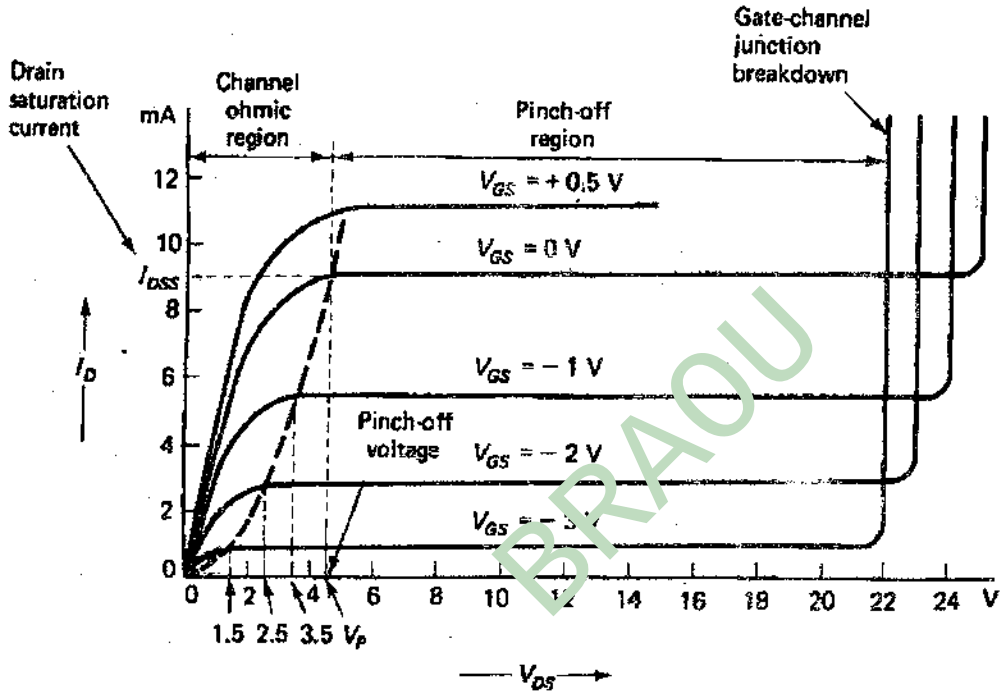


Figure 4.4 n-Channel IFET drain output characteristics

The channel continues to behave as an almost constant resistance, until the voltage drop along it becomes large enough to cause considerable penetration by the depletion regions. At this stage the channel resistance is significantly affected by the depletion regions. Further increases in V_{DS} produce smaller increases in I_D, which, in turn, cause increased penetration by the depletion regions and further increase the channel resistance.

Because of the rapid increase in channel resistance at this stage (produced by increasing I_D), a saturation level of I_D is reached, where further increases in V_{DS} produce only very slight increases in I_D. The drain current at this point, with V_{CS} at zero, is referred to as the drain-source saturation current I_{DSS} (see Fig. 4.4). When the drain current saturation level is reached, the shape of the depletion regions is such that they appear to pinch off the channel. For this reason, the drain source voltage at which I_D levels off is designated the pinch-off voltage (V_S), as indicated in Fig.4.4. The region of the characteristic where I_D is fairly constant is referred to as the pinch-off region. With continued increase in V_{DS}, a voltage will be reached at which the gate channel junction breaks down. This is the result of the charge carriers which make up the reverse saturation current at the gate channel junction being accelerated to a high velocity and producing an avalanche effect. At this point the drain current increases very rapidly, and the device may be destroyed. The normal operating region of the characteristics is the "pinch-off region."

4.2.1 Output or drain characteristics

When an external bias of, say, — 1 V is applied between the gate and source, the gate channel junctions are reverse biased even when I_D = zero. Therefore, when $V_{DS} = 0$ the depletion regions are already penetrating the channel to some extent. Because of this, a smaller voltage drop along the channel (i.e., smaller than when $V_{GS} = 0$) will increase the depletion regions to the point at which they pinch off the current. Consequently, the pinch-off voltage is reached at a lower I_D than when V_{GS} =0. The characteristic for —1V is shown in Fig. 4.

By employing several values of negative external bias voltage, a family of I_D,V_{DS} characteristics is obtained as shown in Fig. 4.4. Note that the value of V_{DS} for breakdown is reduced as the negative gate bias voltage is increased. This is because V_{GS} is adding to the reverse bias at the junction.

If on the other hand a positive gate bias voltage is applied, a larger I_D will result, as shown by the characteristic for V_{GS} = +0.5V in Fig. 4. In general, however, V_{GS} is maintained negative to avoid the possibility of forward biasing the gate channel junctions.

The drain resistance 'r_D' can be calculated from the drain (output) characteristics as

$$r_D = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}=Constant} \qquad \ldots(4.1)$$

4.2.2 Transfer Characteristics

The FET transfer characteristics are experimentally determined by maintaining V_{DS} at a constant level and varying V_{GS} in convenient steps. At each step of V_{GS} the I_D and V_{GS} levels are recorded, and a table of values is obtained from which a graph of I_D versus V_{GS} is plotted. This results in asset of transfer characteristics then, the variation of I_D with V_{GS} for different values of V_{DS} are in Fig 4.

The transconductance of the FET can be calculated from the transfer (mutual) characteristics with the relation

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=Constant} \qquad \ldots(4.2)$$

The drain source saturation current (I_{DSS}) the pinch-off current, and the pinch-off voltage (V) and are connected the relation (4.3). The amplification factor μ can be calculated from the values of r_d and g_m from relation (4.4).

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \qquad \ldots(4.3)$$

$$\mu = r_D\, g_m \qquad \ldots(4.4)$$

The operation of the p-channel FET is exactly identical to that of an n-channel FET except for the change in polarity of the biasing voltage to be reversed. The characteristics of the p-channel FET are also similar to that of an n-channel FET.

4.3 THE TUNNEL DIODE

When the concentration of impurity atoms in a p-n diode is very high (say, 1 part in 10^3), the depletion layer is reduced to about 100 A^0. According to the Classical mechanics a carrier must have energy at least equal to the potential-barrier height in order to cross the junction. However, quantum mechanics indicates that there is a nonzero finite probability that a particle may penetrate through a barrier as thin as that indicated above. This phenomenon is called tunneling, and hence these high-impurity-density p-n devices are called tunnel diodes, or Esaki diodes after their inventor.

4.3.1 Energy-band Structure of a Highly Doped p-n Diode

The condition that the barrier thickness be less than $100A^{O}$ is a necessary but not a sufficient condition for tunneling. It is also required that occupied energy states should exist on the side from which the electron tunnels and that allowed empty states should exist on the other side (into which the electron penetrates) at the same energy level. Hence we must now consider the energy-band picture when the impurity concentration is very high. The Fermi level E_F lies inside the forbidden energy gap to make tunneling possible.

$$E_{cn} = E_F + KTln \qquad \ldots(4.5)$$

$$E_{VP} = E_F - KTln \qquad \ldots(4.6)$$

Since $N_C \cdot 10^{19}$ cm^3, then, for donor concentrations in excess of this amount ($N_D > 10^{19}$ cm^3, corresponding to a doping in excess of 1 part in 10^3), in (N_C/N_D) is negative. Hence $E_F > E_0$, and the Fermi level in the n-type material lies in the conduction band. By similar reasoning we conclude that, for a heavily doped p region, $N_A > N_V$, and the Fermi level lies in the valence band. If $E_O > E_G$, so that the contact difference of potential energy E_0 now exceeds the forbidden-energy-gap voltage E_G.

Hence, under open-circuit conditions, the band structure of a heavily doped p-n junction must be as pictured in Fig. 4.6(a). The Fermi level E_F in the p side is at the same energy as the Fermi level E_F in the n side. Note that there are no filled states on one side of the junction, which are at the same energy as empty allowed states on the other side. Hence there can be no flow of charge in either direction across the junction, and the current is zero, an obviously correct conclusion for an open-circuited diode.

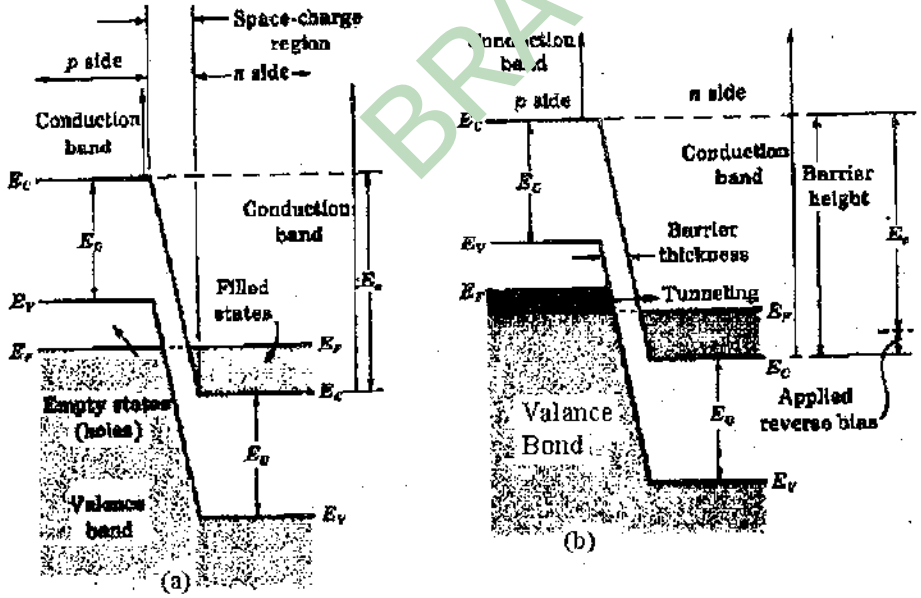


Fig 4.5 Energy bands in a heavily doped p-n diode (a) under open – circuited conditions and (b) with an applied reverse bias. (These diagrams are strictly valid only at 0^0 K , but are closely approximate at room temperature)

4.3.2 Characteristics of a Tunnel Diode

The Volt-Ampere Characteristic With the aid of the energy-band picture of and the cancel of quantum-mechanical tunneling, the tunnel-diode characteristic of may be explained. Let us consider that the material is grounded and that a voltage applied across the diode shifts the side potential with respect to the p side.

(i) Under Reverse Bias:

For example, if a reverse-bias voltage is applied, the height of the barrier is increased above the open-circuit value E_0. Hence the n-side levels shift downward with respect to the p-side levels, as indicated in Fig 4.6(b). We now observe that there are some energy states (the heavily shaded region) in the valence band of the p side which lie at the same level as allowed empty states in the conduction band of the n side. Hence these electrons will tunnel from the p to the o side, giving rise to a reverse diode current. As the magnitude of the reverse bias increases, the heavily shaded area grows in size, causing the reverse current to increase, as shown is by section 1 (A.O) Fig 4.8. Thus the tunnel diode behaves as an excellently good conductor under reverse bias. This is clearly shown in the part of the characteristics curve (AO) shown in Fig.4.8.

(ii) Under Forward Bias

Consider now that a forward bias is applied to the diode so that the potential barrier is decreased below E_O. - Hence the n-side levels must shift upward with respect to those on the p side, and the energy-band picture for this situation is indicated in Fig. 4.7(a) It is now evident that there are occupied states in the conduction band of the n material (the heavily shaded levels), which is at the same energy as allowed empty states (holes) in the valence band of the p side. Hence electrons will tunnel from the n to the p material, giving rise to the forward current of Fig. 4.8.

As the forward base is increased further, the condition is reached. Now the maximum number of electrons can leave occupied states on the right side of the junction, and tunnel through the barrier to empty states on the left side, giving rise to the peak current I_P in Fig. 4.8. If still more forward bias is applied, the situation in Fig4.7(c) is obtained Fig 4.7. This is shown by the part of the characteristics curve OB shown in Fig 4.8. The energy – band diagrams in a heavily doped p-n diode for a forward bias. As the bias is increased, the band structure changes progressively fro[illegible] (a) and (d) Fig. 4.8 the tunneling diode is shown solid.

The injunction current is the da[illegible]hed curve. The sum of these two gives the tunnel-diode volt-ampere characteristi[illegible], which is shown in (b) and the tunneling current decreases, giving rise to section B[illegible] of Fig.4.8

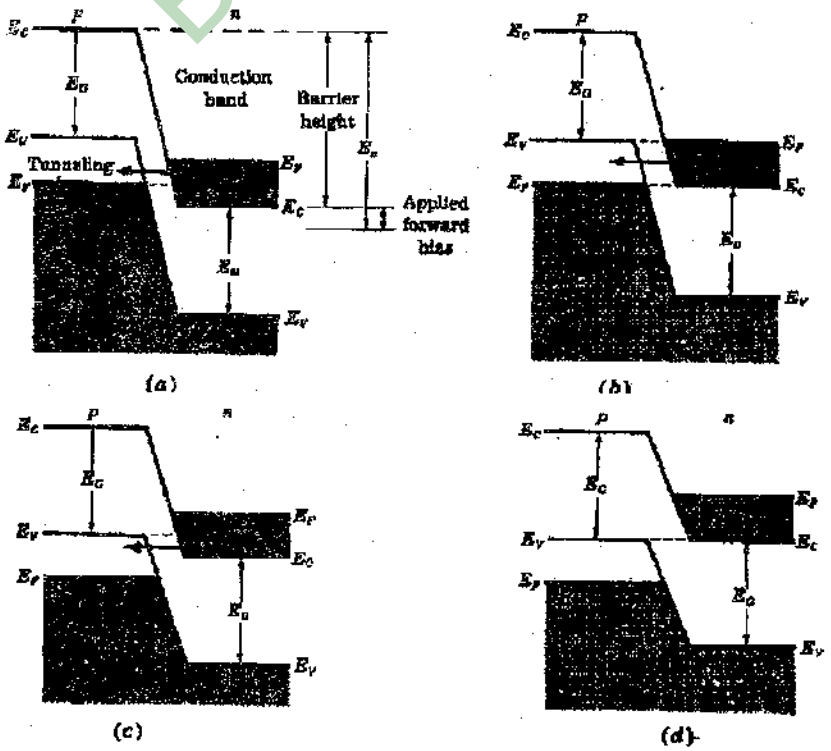


Fig. 4.6 The energy-band diagrams in a heavily doped p-n diode for a forward bias. As the bias is increased, the band structure changes progressively from (a)

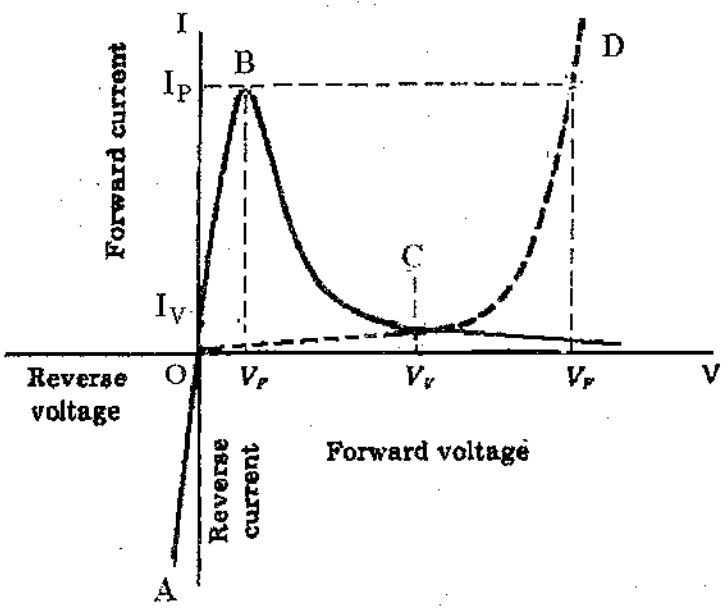


Fig. 4.7 The tunneling current is shown solid. The injection current is the dashed curve. The resultant of these two curves for the tunnel-diode volt-ampere characteristics is shown as curve AOBCD.

Finally, at an even larger forward bias, the band structure of Fig. 4.7(d) is valid. Since now there are some empty allowed states on one side of the junction at the same energy as occupied states on the other side, the tunneling current must drop to zero.

In addition to the quantum-mechanical current described above, the regular p-n junction injection current is also being collected. This current is indicated by the dashed section CD of Fig. 4.8. The curve in Fig.4.8 is the sum of the solid and dashed curves of Fig. 4.8, and this resultant is the tunnel-diode characteristic of Fig. 4.8.

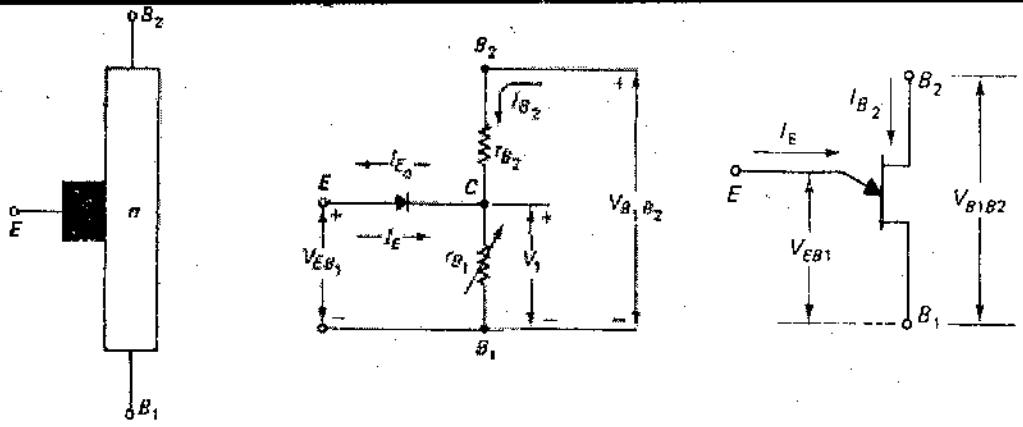
The most important part of the characteristics curve is BC in Fig.4.8. Which shows negative resistance with in this region. This is used in designing UHF amplifiers and oscillators

4.4. THE UNI JUNCTION TRANSISTOR

The operation of a unijunction transistor (UJT) is quite different from that of bipolar BJT and field effect transistors (FET) although it is also a three-terminal device. The input resistance of the device between its emitter and base -1, rapidly decreases when the input voltage reaches a certain level. This is termed as a negative resistance and it is this special characteristic, which makes the UJT useful in designing several special circuits like relaxation oscillators and timing circuit etc.

Basically, the unijunction transistor (also known as a double-based diode) consists of a bar of lightly doped n-type of silicon bar with a small piece of heavily doped p-type material joined to one side. The concept is illustrated in Fig4.9. The end terminals of the bar are designated Base 1 (B_1) and Base 2 (B_2), and the p-type region is termed the emitter (E). Since the silicon bar is lightly doped it has a high resistance, and it can be represented as two resistors, r_{B1} between B_1 are C and r_{B2} from B_2 to C as shown in Fig. 4.9(b). The sum of r_{B1} and r_{B2} is designated R_{BB}. The circuit symbol for a UJT is shown in Fig. 4.10. The arrowhead points in the direction of the conventional current flow for a forward-biased junction. In this case it points from the p-type emitter to the n-type bar or channel. The voltages polarities and current directions for operation of the device are also shown in fig.4.9 (b, c). Constructional Details of Uni-Junction Transistor (UJT) are shown in Fig. 4.9

A plot of emitter voltage (V_{EB1}) versus emitter current (I_E) gives the emitter characteristics shown in Fig. 4.10



(a) Basic construction (b) Equivalent circuit (c) Circuit Symbol.

Figure 4.8. Basic construction and equivalent circuit of Uni-Junction Transistor (UJT).

The p-type emitter forms a pn-junction with the n-type silicon bar, and this is represented as a diode in the equivalent circuit Fig 4.9(b). With a voltage V_{B1B2} applied as shown, the voltage at the junction of r_{B1} and r_{B2} is given by

...(4.7)

=

where $R_{BB} = r_{B1} + r_{B2}$ and = called the intrinsic stand off ratio. ...(4.8)

4.4.1 Operation of UJT and its characteristics:

(a) If V_1 is also the voltage at the cathode of the diode representing the pn-junction, while the emitter terminal is open circuited, the only current flowing in the device is

...(4.9)

(b) If the emitter terminal is grounded, the pn-junction diode is reverse biased and a small emitter current as saturation known as reverse current (I_{E0}) flows in to the emitter. This is represented by the point A on the characteristic curve is shown in Fig. 4.10.

(c) Now consider what happens when the emitter input voltage (V_{EB1}) is slowly increased from zero. As V_{EB1} becomes equal to V_1, I_{EO} will be reduced to zero. With equal voltages on either side of the diode, no reverse current or forward current will flow through the device. This is represented by point B on the characteristics curve.

(d) Beyond the valley point since all the charge carriers available conduction are point in conduction no more charge carriers are left out. Hence the device exhibits saturation beyond point 'O' this is shown by the characteristics curve D.E.

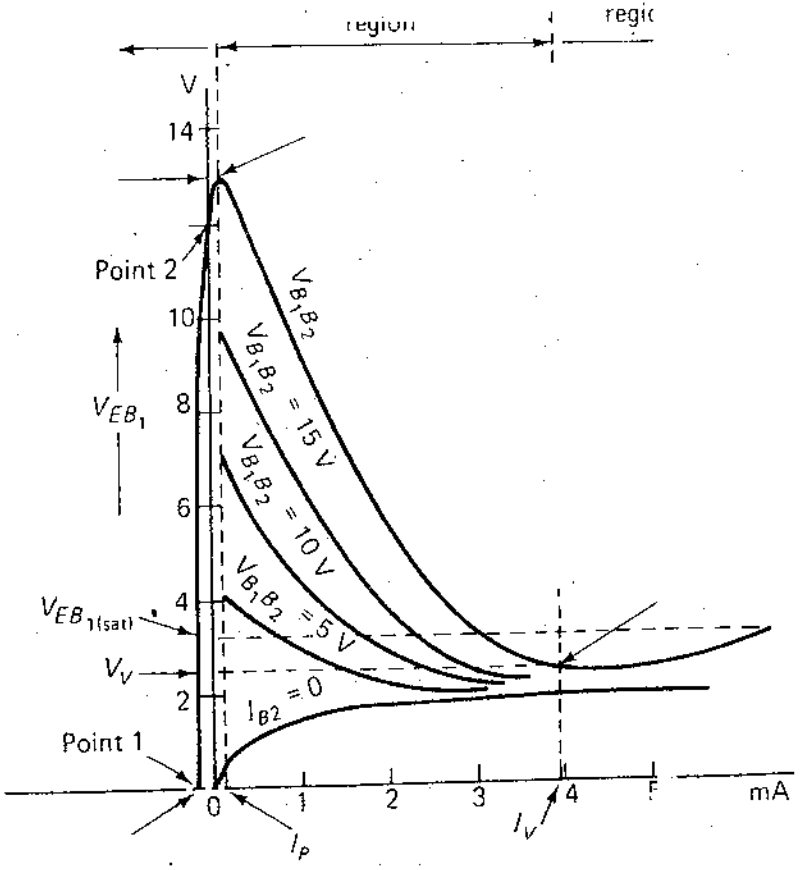


Fig 4.9. UJT emitter characteristics.

(e) With a further increase in V_{EB1} the pn-junction becomes forward biased, and a forward emitter current I_E begins to flow from the emitter terminal into the n-type silicon bar. When this occurs, charge carriers are injected into the r_{B1} region of the bar. Since the resistance of a semiconductor material is dependent upon the number of charge carriers, the additional charge carriers injected into the region cause the resistance of the r_{B1} region to rapidly decrease. With decrease this causes the voltage at the Kathode of the diode to decrease in resistance, the voltage drop across r_{B1} also decreases, causing the pn-junction to be more heavily forward biased. This result in a greater forward current, and consequently more charge carriers are injected causing still further reduction in the resistance of the r_{B1} region. The input voltage drop across r_{B1} is also "pulled down," and the input current (D) is increased to a limit determined by the source resistance. The device remains in this ON condition until the input is opening circuited or until the current I_E is reduced to a very low level. This is represented by the section of the characteristics curve is represented by CD. This point is known as valey point.

Increasing V_{EB1} beyond this point begins to forward bias the emitter junction. At the peak point where $V_{EB1} = V_1$ the junction is just forward biased, and a very small forward emitter current is flowing. This is termed the peak current represented by point C on the characteristics. Up until this point, the UJT is said to be operating in the cutoff region.

This negative resistance region is the most important region on the characteristics of the UJT. When V_{BB} is reduced below 20 V, V_1 will also be reduced and the UJT will switch on at a lower value of V_E. Thus, using various levels of V_{BB}, a family of V_{EB1} / I_E characteristics for a given UJT can be plotted as shown in Fig. 4.10.

4.5 THE SILICON CONTROLLED RECTIFIER

4.5.1 Construction and working of SCR:

The silicon-controlled rectifier (SCR) can be thought of as an ordinary rectifier with

a control element. The current to the control element, which is termed as the gate, determines the anode-to-kathode voltage at which the device commences to conduct. The gate bias may keep the device OFF, or it "may permit conduction" to commence at any desired point in the forward half-cycle of a sinusoidal input. The SCR is widely employed as an ac power control device. Many other devices, such as the DIAC, TRIAC, etc., are based on the SCR principle. Collectively, SCR-type devices are known as "**Thyristors**". This term is derived from thyratron and transistor, the thyratron being a gas-filled tube, which behaves like an SCR.

Figure 4.11(a) shows why an SCR is sometimes referred to as a four-layer device or pnpn device. The SCR consists of four layers of semiconductor material, alternately p-type and n-type layers stacked. The layers are designated p_1, n_1, p_2, and n_2 in as shown Fig. 4.11(a). Three junctions are produced: J_1,J_2 and J_3, and there are three terminals, anode (A), Kathode (K), and gate (G).

To understand the operation of the device, it is necessary to imagine layers n_1 and p_2 are split into n_1, ,P_2, and , as shown in Fig.4.11(b). Since n_1 is connected to , and p_2 is connected to , this has not really changed anything. However, it is now possible to think of p_1, n_1, as a pnp transistor, and , p_2, n_2 as an npn transistor. Replacing the transistor block representations in Fig.4.11(b) with the pnp and npn circuit symbols gives the two-transistor equivalent circuit Fig. 4.11(c). It is seen that Q_2 collector is connected to Q base, and the Q_1 collector is commoned with Q_2 base. The Q_1 emitter is the SCR Anode terminal, the Q_2 emitter is the Kathode, and the gate is the junction of the Q_1 collector and the Q_2 base. The circuit symbol for the SCR is shown in Fig. 4.11(d).

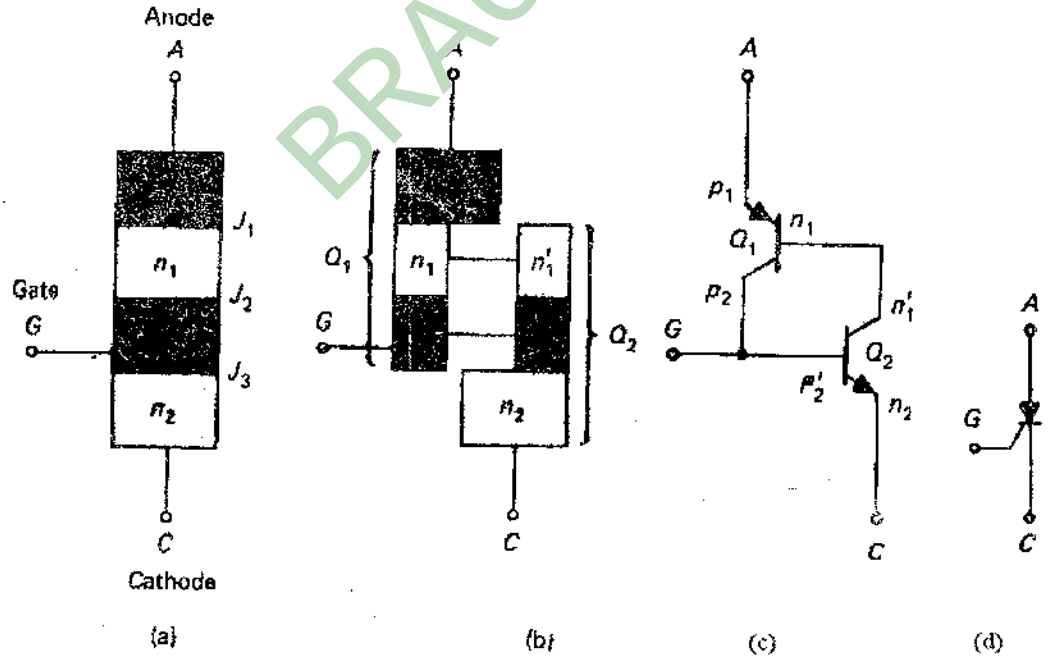


Figure4.10. (a) and (b) SCR basic construction; (c) Two-transistor equivalent circuit of SCR; (d) Schematic symbol of SCR.

To forward bias the SCR, a voltage is applied as shown in Fig. 4.12(a), positive on the anode, negative on the kathode. If the gate is left unconnected, only small leakage currents flow and both transistors remain cut off. Reference to Fig.4.11(a) shows that the even through junction d J_1 and J_3 are forward bias junction J_2 is reverse biased,. Hence, only small leakage currents flow through the device.

When a negative gate—Kathode voltage is applied, the Q_2 base—emitter junction is reverse biased, and only small leakage currents flow, so both transistors remain off.

This positive bias junction J_2 also a positive gate Kathode voltage Fig.4.12(b) forward biases the Q2 base emitter junction and causes a base current 'B_2' to flow, consequently producing collector current 'I_{C2} Since 'I_{C2}' is the same as 'B_1'also switches on and I_{B1} flows Q_1 also switches ON,and I_{C1} flows, providing base current I_{B2}. Each collector current provides much more base current than is needed by the transistors, and even when the gate current (I_{G1}) is cut-off the transistors remain in an ON state, conducting heavily with only a small SCR anode-to-kathode voltage drop. The ability of the SCR to remain in ON state even when the triggering current is removed is referred to as "Latching". To switch the SCR on, only a short pulse of gate current is required. Once switched ON, the gate has no further control, and the device remains ON until the anode—kathode voltage is reduced to near zero.

The SCR can also be triggered ON with the gate open circuited, if the anode-to-kathode voltage is made large enough. Consider Fig. 4.11(a) again. With a forward bias (positive ON A, negative on C), junctions J_1 and J_3 are forward biased while junction J_2 is reverse biased. When V_{Fe} is made large enough, J_2 will break down due to avalanche effect. The resultant current flow across the junction constitutes collector current in each transistor. Each collector current again feeds base current into the other transistor, and both transistors switch ON.

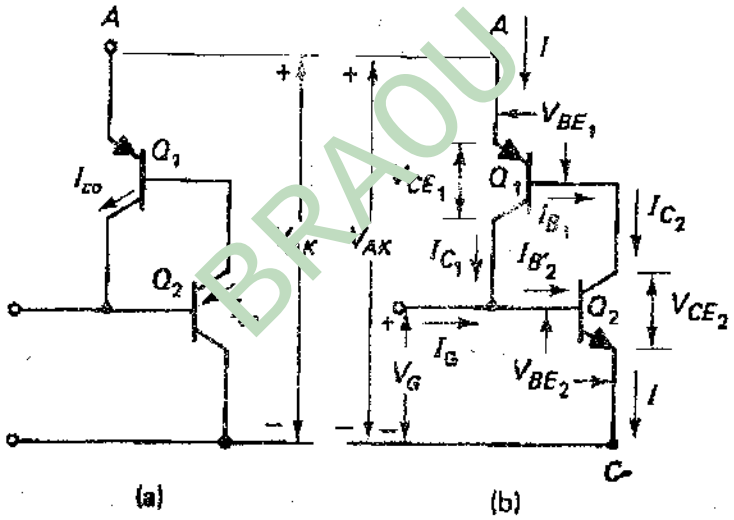


Fig.4.11 SCR Operations

4.5.2 Characteristics of SCR:

Typical forward and reverse characteristics for an SCR are shown in Fig. 4.13. First consider the reverse characteristics, and refer again to Fig.4.11(a). When a reverse bias is applied (negative on A, positive on K), J_2 is forward biased while J_1 and J_3 are reverse biased. When the reverse voltage V_{AK} is small, a reverse leakage current (I_{C1}) flows (see Fig.4.13). This is typically around 100 A and is sometimes referred to as the reverse blocking current. As the level of reverse voltage is increased, I_{RX} remains approximately constant until V_{AK} becomes large enough to cause J_1 and J_3 to break down. As shown in Fig.4.13, the reverse current increases very rapidly when the reverse breakdown voltage is reached, and if I_R is not limited the device would be destroyed. The region of the reverse characteristics before reverse breakdown is termed the reverse blocking region.

When the SCR is forward biased with I_G=0, two junctions (J_1 and J_3) are forward biased and J2 is reverse biased. With small anode-to-kathode voltages (+V_{AK}), a small leakage current flows (Fig. 4.13). This forward leakage current (I_{FX}) is approximately

equal to I_{RX} and has a typical value of 100 A. With I_G at zero, I_F remains at I_{FX} until V_{AK} is made large enough to cause the reverse-biased J_2 junction to break down. The forward voltage at this point is termed the forward break over voltage VF(BO). When VF(BO) is reached, the two component transistors Q_1 and Q2 are immediately switched ON into saturation as already explained, and the anode—kathode voltage falls to the forward conduction voltage (V_F).

So far the forward characteristics have been discussed only for the case of I_G =0. Now consider the effect of I_G greater than zero. As already shown, when + V_{AK} is less than V_{FBO}(BO) and I_G is zero, a small leakage current flows. This is too small to have any effect on the level of V_{AK} at which switch ON occurs. When I_G is made just slightly larger than the junction leakage currents, it will have a negligible effect ON the level of +VAK for switch-ON; see I_{G1} in Fig.4.13. Now consider the opposite extreme. When I_G is made larger than the minimum base current required to switch Q2 ON, the SCR remains on OFF state until +V_{AK} is large enough to forward bias the base-emitter junctions of Q_1 andQ_2. This is illustrated in Fig 4.13 where it is seen that when 'I_G = I_{G4} switch ON occurs when + V_{AK} reaches the relatively low voltage of V_4.

Between I_{G1} and I_{G4} there are gate current levels which permit device switch ON at levels of + VAK greater than V_4 but less than V_{FBO}(BO).

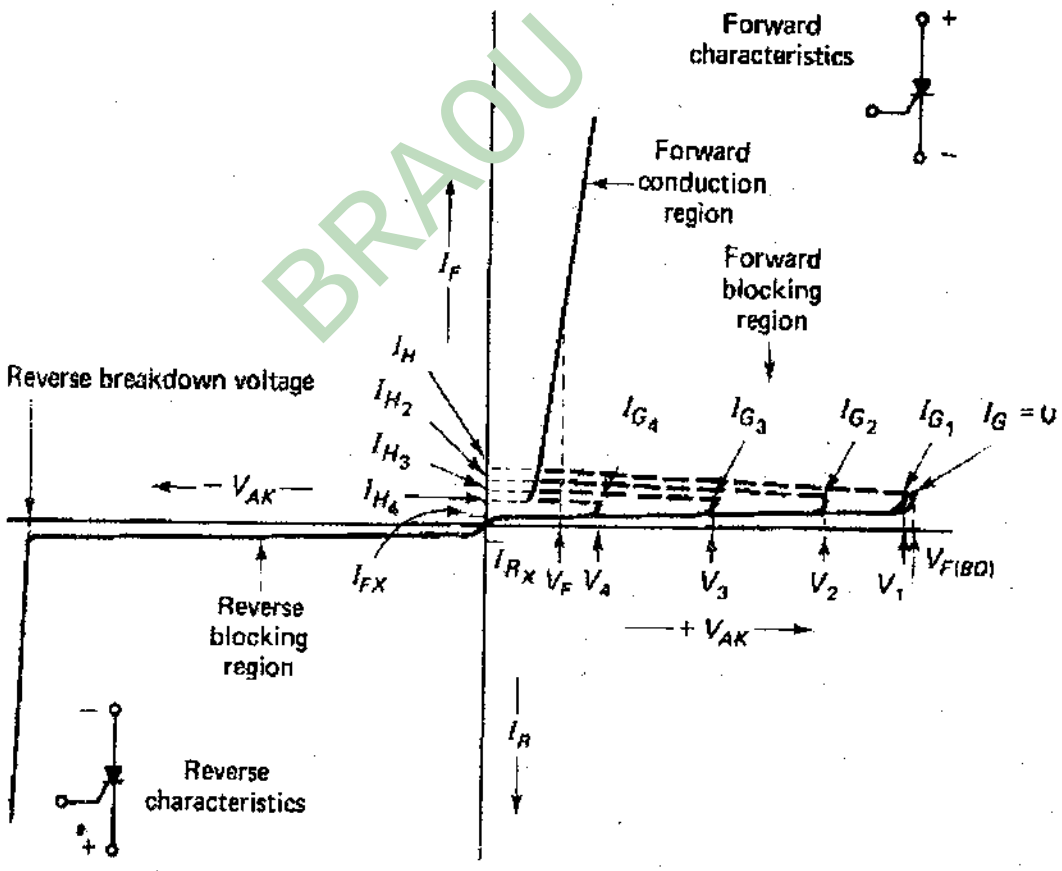


Fig. 4.12 SCR Forward and reverse characteristics

The forward conduction voltage (V_F) is made up of (V_{BE1} + V_{CE2}) or (V_{BE2} + V_{CE1}) Fig.4.12(b). The value of V_{CE} for a transistor biased on in saturation is typically about 0.2 V, and since forward V_{BE} for a silicon transistor is about 0.7 V, the total value of V_f is around 0.9 V. The region of the forward characteristics before switch ON occurs is known as the "forward blocking region", and the region after switch ON is termed the "forward conduction" region. In the forward conduction region, the SCR is behaving as a forward-

biased rectifier.

To switch an SCR off, the forward current (I_F) must be reduced below a level known as the holding current (I_H) (Fig. 4.13). The holding current is the minimum level of I_F that will maintain the SCR conducting. If a gate current (I_G) greater than zero is maintained while the SCR is on, lower values of holding current (I_{H2}, I_{H3} or I_{H4}) are possible. Manufacturers usually specify I_H asl I_{HO} the holding cur rent with the gate open circuited, or I_{HX} the holding current with a specified bias resistance connected between gate and kathode.

4.6 TRIAC AND DIAC

4.6.1 TRIAC:

The construction, equivalent circuit and characteristics of a TRIAC are shown in Fig. 4.14. The device amounts to two inverse parallel connected SCR's with a common gate terminal. Section n_1, p_2, n_3, and p_3 in Fig. 4.14(a) form one SCR, which can be represented by transistors Q_1 and Q_2 in Fig. 4.14(b). Similarly, p_1, n_2, p_2, and n_4 form another SCR, which has the transistor equivalent circuit Q_3 and Q_4. P_2 is the layer common to both SCR's, and it functions as a gate for both devices. Because of the inverse parallel connection, the other terminals cannot be identified as anode and cathode; instead they are designated A_1 and A_2.

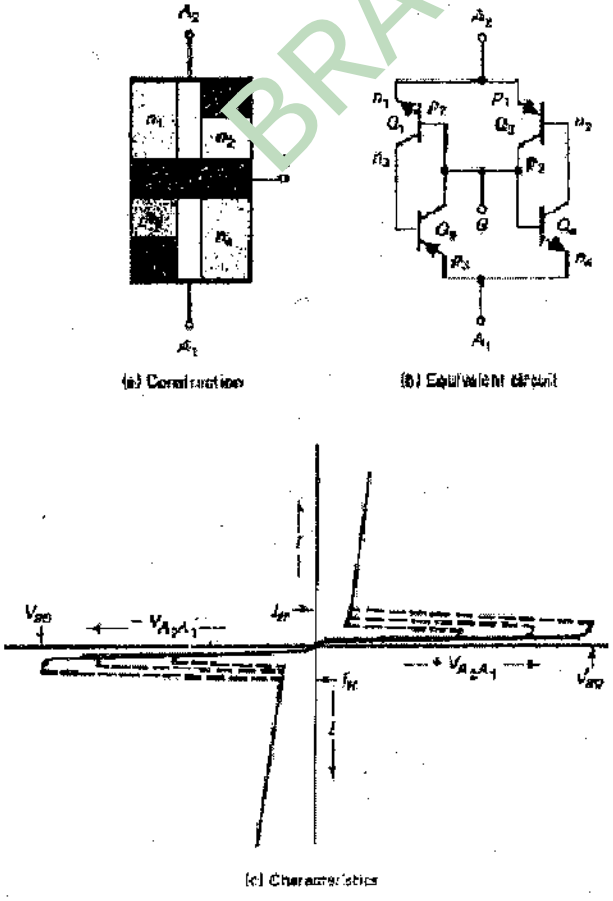


Fig 4.13

When the gate is made positive with respect to A_1, and A_2 is also made positive with respect to A_1, transistors Q_3 and Q_4 switch on [Fig. 4.14(b)]. In this case A_2 is the anode

and A_1 is the cathode. When the gate and A_1 are made positive with respect to A_2, Q_1 and Q_2 switch on. Now A_1 is the anode and A_2 the cathode. It is seen that the TRIAC can be made to conduct in either direction. No matter what the bias polarity, the characteristics for the TRIAC are those of a forward-biased SCR [Fig. 4.14 (c)].

4.6.2 DIAC:

DIAC is Aimply a TRIAC without a gate terminal. Switching on the device is effected by raising the applied voltage to the breakover voltage. The DIAC symbol and the characteristic curves are shown in Fig 4.15(a,b).

Applications:

The SCR is useful for controlling the current through any load thuring the positive half cycle. The TRIAC and DIAC are useful for controlling current through load during both the half cycles. All these devices are used for light dimmers, motor speed control, leather temperature regulation, and battery charges etc.

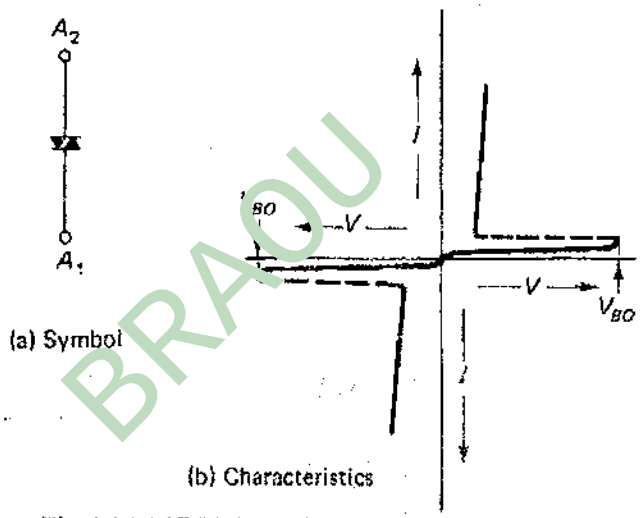


Fig 4.14 (a)DIAC symbol (b) Characteristics

4.7 SUMMARY

In the special semiconductor devices, the negative resistance property of the tunnel diode and UJT are made use of in designing oscillators.

The field effect transistor has advantages of having high input impedance, high power gain and low noise. Silicon controlled rectifier shows controlled rectifying property.

4.8 SAMPLE EXAMINATION QUESTIONS

I. Answer the following question in detail.

1. Explain the tunneling phenonmenon with help of a energy band diagram. What are the key parameters of a tunnel diode?

II. Answer the following questions briefly.

1. Write a short note on the Field Effect Transistor

2. What are the unique characteristics of a tunnel diode?

III. Solve the following problems.

1. Assume that the barrier potential for a diode is 0.63 V at room temperature (25°C). If the temperature increases to 80° C, what is the barrier potential at the new temperature
   [Ans: 0.49V]

2. A germanium diode for which saturation current Is = l0A, is conducting 2 mA at room temperature. What is the forward voltage drop?
   [Ans: 0.14 V]

3. A transistor has an (Alpha) of 0.98. For an emitter current of2 mA calculate the base current I_B Also calculate
   [Ans : 1.96 mA; (=49]

4. A transistor has a of 60. find [Ans: 0.984]

5. Find I_{CE} as a function of lea and , using the transistor equation $I_{CE} + I_{CBO}$ A transistor has an I_{CBO} = 40 A when measured in the common base configuration. If = 100 find I_{CE} [Ans: 5mA]

6. Sketch the curve vs or between 0.95 and 1.00 in steps of 0.01. Comment on the plot obtained. Use the value of in problem 5 and find out the corresponding value of

4.9 REFERENCES

1. Semiconductor devices and Circuits	Jacob Millman and C.C. Halkias
2. Integrated Electronics – Analog and Digital Circuits	Jacob Millman and C.C. Halkias
3. Fundamentals of Electronic Devices	David Bell A
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4.10 GLOSSARY

Bias portion	: A Voltage applied to an electronic device to determine the of The Characteristic of the device at which operates.
Microwave	: An electromagnetic wave with a wavelength in the approximate range 1 mm to 0.3 m. i.e. between infared radiation and radio waves (Radar uses these wavelengths).
Negative resistance	: In certain devices the point at which the voltage current has a Negative slope. Le the current decreases as the voltage increases. Such devices include tunnel diode UJT etc.

BLOCK – II

TRANSISTOR AMPLIFIERS

UNIT 5: TRANSISTOR BIASING AND LOAD LINE ANALYSIS

Contents:

5.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

1) Biasing a transistor

2) Schemes of biasing and

3) Load line analysis

After going through this unit you can explain

1) The working of electronic circuits used in biasing

2) The working of a transistor amplifier and

3) Fixing quiscent of operating point –Q using load line

5.1 INTRODUCTION

The bipolar junction transistor (BJT) functions as a linear device when its operation is limited to the active region of its characteristic. To establish a quiscent operating point –Q in this region it is necessary to apply appropriate direct potentials and currents. With no signals applied to the base, the collector current and voltage determine a point approximately in the centre of the output characteristics, with zero base excitation the operating point is called the quiescent point Q. Biasing is the procedure to establish and maintain an quiescent operating point of the circuit.

5.2 TRANSISTOR CURRENT COMPONENTS

Figure 1.5 shows the various current components, which flow across the forward biased emitter junction and reverse biased collector junction.

1. The emitter current consists of electron current I_{nE} and hole current I_{pE}. The ratio of hole to electron current crossing the emitter junction is proportional to the ratio of the

conductivity of the 'P' type to 'n' type material.

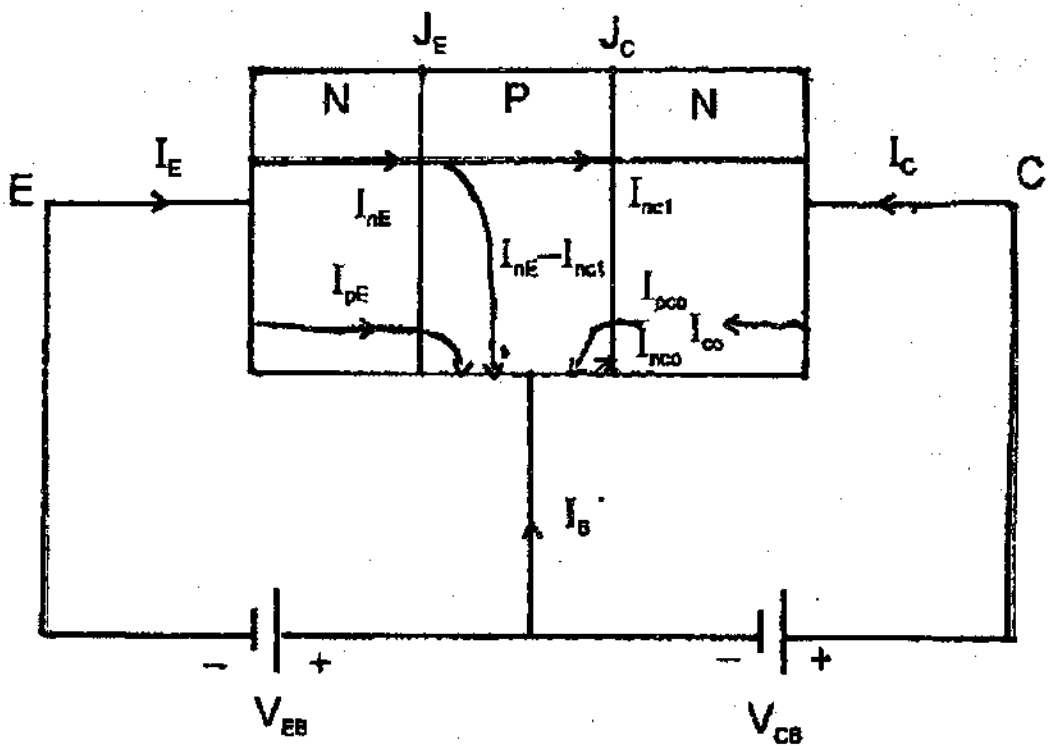


Fig. 5.1 Transistor current components (NPN) for forward biased emitter junction and reverse biased collector junction

2. In practice, the doping of the emitter is made much larger than the doping of the base. This feature ensures that the emitter current is entirely due to majority carriers.

3. Let $I_{pn}(O)$ and $I_{np}(O)$ are the respective minority carrier diffusion currents of I_{PE} and I_{nE}. Hence the total minority carrier current $I = I_{pn}(O) + I_{np}(O)$

   Total majority carrier current at the emitter is $I_E = I_{PE} + I_{nE}$

4. Not all the majority carriers crossing the emitter-base junction J_E reach the base-collector junction, because some of them combine with the minority carriers in the base region.

   Let I_{PCI} = hole current at J_C as a result of holes crossing the base from the emitter [for PNP transistor]

   I_{nc1} = electron current at J_C as a resulting electrons crossing the base from the emitter [for NPN transistor].

5. Under emitter open circuit condition, the collector junction remains reverse biased. The I_c must equal to the reverse saturation current 'co. This current consists of two components.

   I_{nco}= electron current moving from p to the a region across J_C.

   I_{PCO}= hole current moving from x to the p region across J_C

   hence $-I_{CO} = I_{nCO} + I_{PCO}$

6. Total collector current under emitter junction is forward biased is calculated as follows

$$I_C = I_{CO} - I_{nC1} = I_{CO} - \alpha I_E \qquad \ldots(5.1)$$

where α = fraction of the total emitter current which represents electrons which have travelled from the emitter across the base to the collector.

7. For npn transistor I_E is negative and both I_C and I_{CO} are positive and for pnp transistor these currents are reversed.

8. Large signal current gain (α):-
   The symbol 'α' may be defined as the ratio of negative of the collector current increment
   from cutoff ($I_C = I_{CO}$) to the emitter current change from cutoff $I_E = 0$ or

$$\alpha = -\frac{I_C - I_{CO}}{I_E}$$

   It is also called the large signal current gain of C_B configuration.

   'α' is always positive and its nominal value lies in the range of 0.90 to 0.995. It should be noted that it is not a constant but varies with emitter current I_E collector voltage V_{CE} and temperature.

9. The equation 5.1 is valid only if the emitter is forward biased and the collector is reverse biased. Hence it is need to generalize the equation 5.1 i.e., the collector junction Je needs to be substantially reverse biased. To achieve this generalization we need only replace I_{CO} by the current is a PN diode and V by V_C where V_C represents the drop across J_C. The complete expression for I_C for any V_C and I_E is

$$I_C = -\alpha I_E + I_{CO}\left(1 - e^{V_C/V_T}\right) \qquad \ldots(5.2)$$

The physical interpretation of equation 5.2 is that the PN junction diode current crossing the collector junction is augmented by the fraction 'α' of the current I_E flowing in the emitter.

5.3 THERMAL RUNAWAY

One may use separate batteries for biasing a transistor. This is expensive and inconvenient. It is customary to provide the bias voltages from a single source of power supply. To understand the design of these circuits, called biasing circuits, it is necessary to understand clearly the current flow in transistors.

Consider the NPN transistor shown in Fig. 5.1. The emitter current I_E is the sum of the base current I_B and caused by collector current $\alpha_{fe} I_B$. In spite of the reverse bias, there is a collector-base current I_{CO} caused by the thermally generated minority charge carriers in collector and base regions.

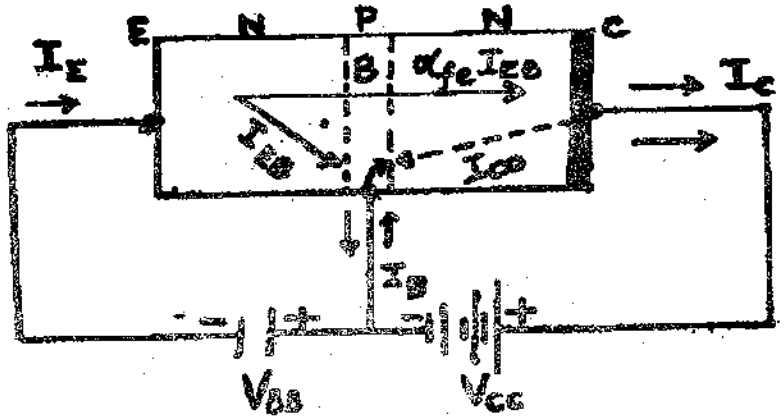


Fig. 5.2. Currents in an NPN Transistor

They drift towards the collector-base junction and constitute I_{CO}. It is called the collector

$$I_C = \alpha_{fe} I_B + I_{CO} \qquad ...(5.3)$$

Because I_{CO} is caused due to the thermal energy, the value of I_{CO} increases rapidly with temperature.

The current I_{CO} tends to develop a bias on the base, which increases the emitter-to-collector current in the transistor. Let us consider the circuit of Fig. 5.1 with base lead disconnected. With base open, there cannot be any net base current. In other words $I_B = I_{CO}$ From Equ. (5.3) if $I_{CO} = 100\,\mu$ A, $\alpha_{fe} = 50$, I_C is 5.1 mA. This collector current increases the temperature of the transistor. This increases I_{CO}, which in turn increases I_C. This process goes on cumulatively and a large current is built up which finally may damage the transistor. This phenomenon is called' thermal runaway'. To prevent thermal runaway, the biasing circuit should be designed properly. Increase in temperature should automatically lead to a decrease in I_B such that I_C is kept constant.

The change in I_C with respect to a change in I_{CO} is called the stability factor.

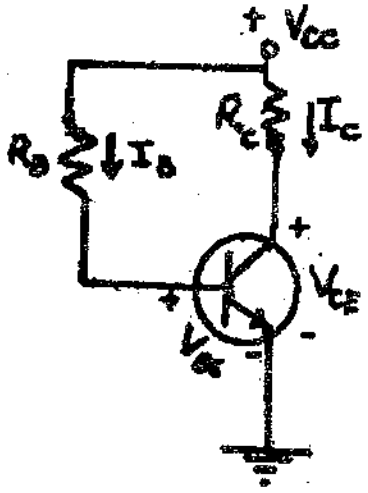
$$S = \text{stability factor} = \frac{dI_C}{dI_{CO}} \qquad ... (5.4)$$

5.4 FIXED-BIAS ARRANGEMENT

One method of biasing the transistor is shown in Fig. 5.3, which is also known as current biasing.

In this circuit, the quiscent base and collector currents are supplied by a single power supply V_{CC}. It biases the emitter-base junction in the forward direction and the collector-base junction in the reverse direction. The voltage V_{BE} will be in the millivolt range and can be neglected in comparison to V_{CC} Thus, the base current

$$I_B \approx \frac{V_{CC} - V_{BE}}{R_B} \approx \frac{V_{CC}}{R_B} \qquad ...(5.5)$$



5.3 Fixed Base Circuit

Since the base current is constant, the circuit is called the fixed-bias circuit.

Substituting $I_C + I_B$ for I_B in Equ. (5.3) and substituting α for α_{fe} we have

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CO}}{I-\alpha} \quad ...(5.6)$$

The stability factor

$$S = \frac{dI_C}{dI_{CO}} = \frac{1}{1-\alpha} \quad ...(5.7)$$

the stability factor is 50 for α =0.98. This indicates that I_C increases 50 times faster than I_{CO} This circuit does not provide a stable operating point.

5.5 SELF-BIAS OR EMITTER BIAS ARRANGEMENT

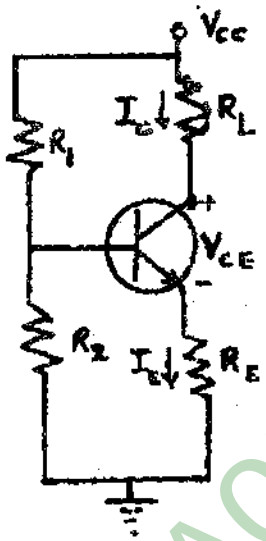


Fig. 5.4 Self bias circuit

The self-bias arrangement shown in Fig. 5.4 provides sufficient protection from thermal runaway. The resistors R_1, R_2, R_E, R_L and the supply V_{CC} provide appropriate bias voltage and currents.

The collector current I_C develops a voltage drop across R_E with the emitter side as positive. When the collector current increases due to rise in temperature, the voltage drop across R_E increases and makes the base terminal less positive. This decreases the base current, which, in turn, decreases the collector current.

Analysis of the self-bias circuit is similar to that adopted for the fixed-bias circuit. The two resistors R_1 and R_2 in the base circuit constitute a voltage divider. The voltage source V_{CC} and R_1 and R_2 may be replaced by the Thevenin equivalent circuit as shown in Fig. 5.5. Where

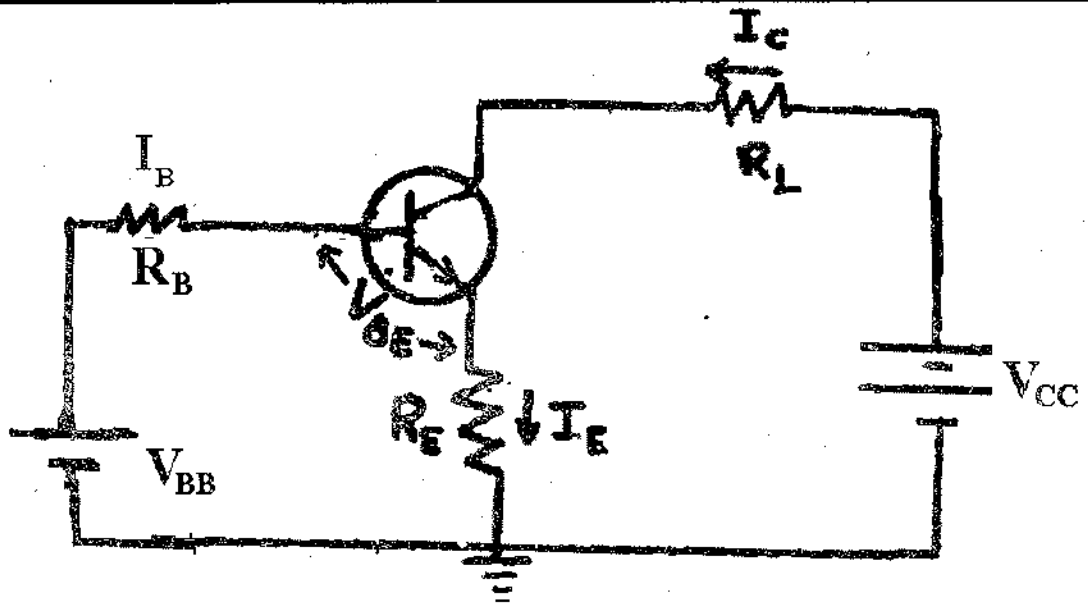


Fig. 5.5. Self-bias; Equivalent Circuit

$$R_B = \frac{R_1 \quad R_2}{R_1 + R_2}$$

and

$$V_{BB} = V_{CC} \frac{R_2}{R_1 + R_2} \qquad \ldots(5.8)$$

Applying Kirchoff's voltage law to the base circuit, we obtain.

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E \qquad \ldots(5.9)$$

Since, ($V_{CE} >> V_{BE}$) neglecting the low value of V_{BE} and substituting $I_B + I_C$ for I_E we get

$$I_B = \frac{V_{BB} - I_C R_E}{R_B + R_E} \qquad \ldots(5.10)$$

Substituting the above value for I_B in Equ. (5.4)

$$I_C = \left(\frac{\alpha}{1-\alpha}\right)\left(\frac{V_{BB} - I_C R_E}{R_B + R_E}\right) + \frac{I_{CO}}{1-\alpha} \qquad \ldots(5.11)$$

$$(1-\alpha)\, I_C = I_{CO} + \frac{\alpha V_{BB}}{R_B + R_E} - \frac{\alpha R_E I_C}{R_B + R_E} \qquad \ldots(5.12)$$

$$I_C = \left(1 - \alpha + \frac{\alpha R_E}{R_B + R_E}\right) = I_{CO} + \frac{\alpha V_{BB}}{R_B + R_E} \qquad \ldots(5.13)$$

$$S = \frac{d I_C}{d I_{CO}} = \frac{1}{1 - \alpha + \frac{\alpha R_E}{R_B + R_E}} \qquad \ldots(5.14)$$

$$S = \frac{\beta + 1}{1 + \frac{\beta R_E}{R_B + R_E}} = \left[\alpha = \frac{\beta}{1+\beta}\right] \qquad \ldots(5.15)$$

if $\frac{R_E}{R_B} << 1$, S = 1 (good stability)

If R_B= 10K Ω R_E = 1 K Ω and β =5.0, we have S= 10 (approx.)

5.6 BJT AS AN AMPLIFIER

Let us now examine how a transistor can be used as an amplifier for time varying signals taking a specific example. The characteristics of an NPN transistor to be used as an amplifier are shown in Fig. 5.5. The bias circuit used is the one shown in Fig 5.2. The values used are Vcc = 18V, RB = 450K Ω and Rc=3k Ω. Assuming V_{BE} negligible as compared to 18V, we get for the Q-point base current.

$$I_{BQ} = \frac{V_{CC} - V_{RE}}{R_B} \approx \frac{V_{CC}}{R_B} \text{ since } V_{BE} << V_{CC} \qquad ...(5.16)$$

$$I_{BQ} = \frac{18v}{450k\Omega} = 40\mu A \qquad ...(5.17)$$

From the base characteristics shown in Fig. 5.5a we get for V_{BEQ} = 0.6V. We are justified in neglecting VBE' considering the circuit of Fig. 5.3, we have.

$$Vcc = I_{CRC} + V_{CE} \qquad ...(5.18)$$

This is called the load line equation. Let us now superpose this load line on the characteristic curves in Fig. 5.5b. Since the load line is a straight line, we need only two points to draw it. The two points chosen are as follows:

Point 1 when V_{CE} = 0 $I_C = \frac{V_{CC}}{R_C} = \frac{18}{3K}$ = 6mA ...(5.19)

Point 2 when Ic = 0, V_{CE} = Vcc = 18 V. ...(5.20)

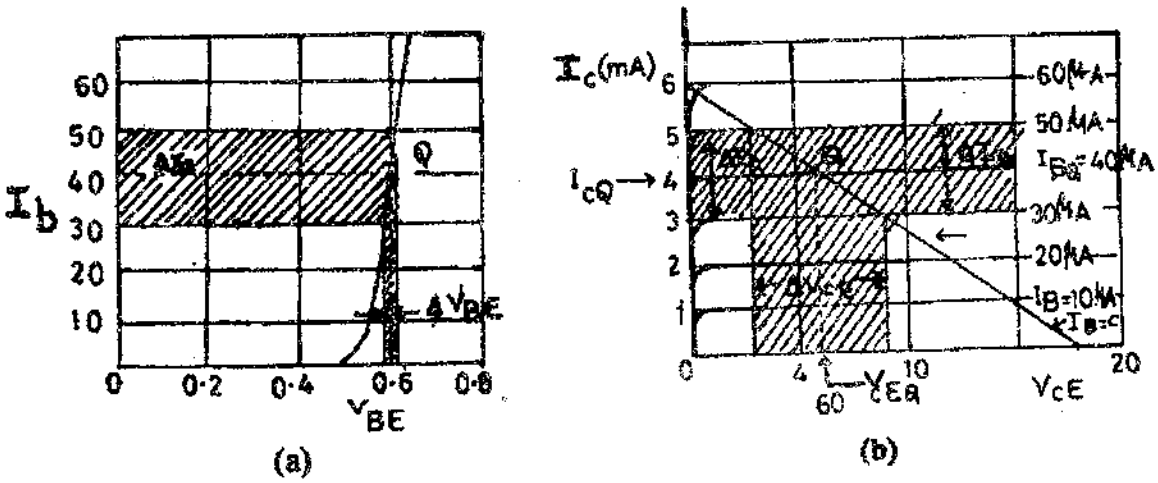


Fig. 5.6 (a) Small variation in V_{BE} results in
(b) Large variation V_{CE}

The two points are marked on the figure and joined by a straight line; it is called the "Load Line". The co-ordinates of a point on the load line gives the current and voltage in the output circuit of a transistor under the given load and bias conditions. The intersection of the load line with I_{BQ} = 40 μ A curve determines the Q-point. The co-ordinates of the Q-point in Fig. 5.6b are

$I_{CQ} = 4$ mA and $V_{CEQ} = 6.5$ V

Now let us assume that the input (base-emitter) voltage varies by 25 mV about 0.6 V. The corresponding variation in the base current, as can be seen from Fig. 6.5a, is 20 μ A i.e. 10 μ A above and below I_{BQ}. This variation I_B leads to a variation of 2mA in the collector current as can be seen from Fig. 5.6. Thus Δ Ic = 2mA and ΔV_{CE}=6V, from this analysis, it can be concluded that a variation of 25 mV in the input circuit has caused a variation of 6V in the output. The amount of voltage amplification, called gain is given by

$$A_V = \frac{6V}{25mV} = 240$$

The graphical analysis described above is an extremely useful technique.

5.7 SUMMARY

Biasing is the procedure to establish and maintain an operating point of the circuit. Two schemes namely fixed bias and self-bias are used in common.

5.8 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail

1. Describe the fixed and self-bias techniques to locate the quiescent operating point of a transistor. Arrive at their Stability Factors.
2. Discuss the effect of negative feedback of an amplifier performance.
3. What does a load line represents?

II. Answer the following questions briefly.

1. What is thermal runaway? Explain
2. The experimental set up shown in 5.4 is used to determine the input resistance of an amplifier. The following are the measured values Vs= 10mV; Vi=5mV with R= IKΩ calculate R_i. [Ans: IKΩ use Equ 5.3]
3. What is the quiescent operating point?

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UNIT-6: AMPLIFIERS - AN INTRODUCTION

Contents:

6.0 AIMS AND OBJECTIVES

This unit explains the concept of an Amplifier and different types of amplifiers with their characteristics.

After going through this unit, you can discuss, the parameters of different types of amplifiers and the method of analysing an amplifier circuit.

6.1 INTRODUCTION

Amplification is the most common process that one comes across in electronic circutary. An amplifier is a circuit, which raises the level of a signal. A small signal at the input is processed to provide at the output, which is identical to the input in all respects except that it is larger in magnitude.

Amplification is accomplished by controlling a power supply-with an element that is actuated by the signal to be amplified. This is illustrated in Fig. 6.1. Thermionic valves, transistors are the most common control elements used in the amplifier.

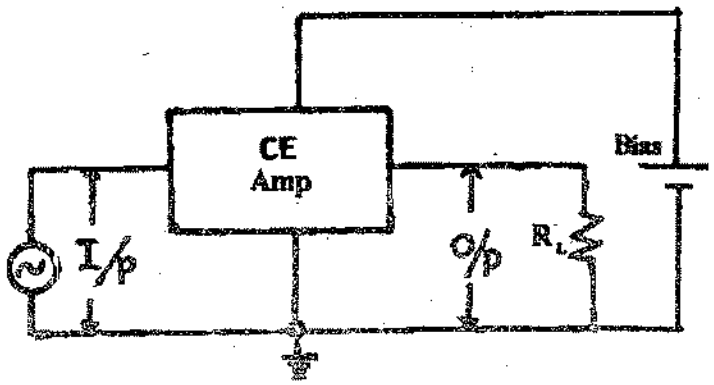


Fig. 6.1. Working of an Amplifier I/P = Input signal CE = Control Element L = Load; PS = Power Supply O/P= Output Signal

The amplifier can be thought of as a black box that has two input terminals, two output terminals and a terminal for supplying DC power as shown in the figure. The signal to be amplified may be DC or AC; Voltage or Current. It delivers some power to the load. Output power is derived from the DC power supply-not from the signal source.

6.2 CLASSIFICATION OF AMPLIFIERS

The type of circuit used in an amplifier depends on the nature of the signal to be amplified and the amount of amplification required. Amplifier Circuits may be classified based on these factors. Many different classifications are possible. They are discussed in this section.

(a) Classification based on the transfer function: The relation between the output and the inut of an amplifier is called the transfer function. The input to an amplifier may be a voltage (V_i) or a current (I_i). Similarly, the output may be voltage (V_O) or current (I_O). This results in four possible combinations of input and output signals. Hence, four types of amplifiers are possible. The four types of amplifiers and their transfer functions are shown in Table 6.1.

TABLE 6.1

Type	Transfer function (A) = $\frac{Output}{Input}$ Or Gain
Voltage	$A_V = V_O/V_i$
Current	$A_i = I_O/I_i$
Transconductance	$G_m = I_O/V_i$
Transresistante	$R_m = V_O/I_i$

(b) Classification based on the method or analysis

It is normally assumed that the gain of the amplifier does not depend upon the amplitude of the input signal. This is true only if the amplifier is operated on the linear part of its characteristic. Such an amplifier is called the linear amplifier. For example, if the amplifier gains are 100 and its input is 5mV, its output will be 0.5V. For the same amplifier, if the input is 50 m V, its output will be 5V. This type of amplifier is called the small signal amplifier i.e., the signal is small enough to confine the operation to the linear part of the characteristic. Under such conditions, the analysis of the amplifier can be carried out using equivalent circuits.

In large-signal amplifiers, the input signal is so large that the device does not operate in the linear part of the characteristics. For example, an amplifier that gives an output signal of l A for an input of 0.1 A, may give an output of 0.8A for an input of 0.2A (gains are 10 and 4). The behaviour of such amplifiers is best analysed graphically. The equivalent circuit analysis does not work here.

(c) Classification based on the frequency range

A single amplifier cannot amplify signals from DC to very high frequencies. Each amplifier caters to a particular, limited frequency range.

The following classification is based on the frequency range of amplification:

DC and LF Amplifiers	:	Amplifies DC and low frequency signals only
Audio frequency(AF) Amps	:	Amplifies signals in the range 20 Hz to 20 KHz
Radio frequency(RF) Amps	:	Amplifies signals in the range 20 KHz to 300 GHz
Video (Wide Band) Amps	:	Amplifies signals from a Video Camera.

(d) Classification based on the types of coupling

In general, the amplification provided by a single stage amplifier is not sufficient. Consequently, two or more stages are cascaded as shown in Fig. 6.2. In such a system, the output of one stage is connected to the input of the next stage by a network, called coupling

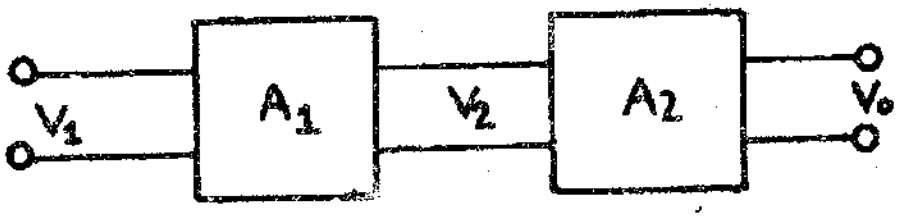


Fig. 6.2 Amplifiers in cascade

A_1 and A_2 are two stages of amplifiers

network. This interstage coupling may be achieved by an R-C network or a transformer. The network couples the A.C signals and decouples the DC voltages. To amplify DC voltage, the coupling has to be a direct one. Based on these considerations, we have direct coupled, Resistance-Capacitance Coupled, and Transformer coupled amplifiers.

(e) Classification based on conduction angle

Amplifiers may be classified on the basis of the conduction angle during which output current flows. Class-A amplifiers have output signals during the complete input-signal cycle. All linear and some power amplifiers are operated under this class. In Class-B amplifiers, the signal current flows for 180^0 of the cycle as in Fig. 6.3. In Class-C operation, output is present only for less than half the input cycle i.e., less than 180^0 of the input cycle. A Class-C amplifier, usually, has a tuned circuit as a load. It is characterised by high efficiency. Its applications include radio and television transmitters.

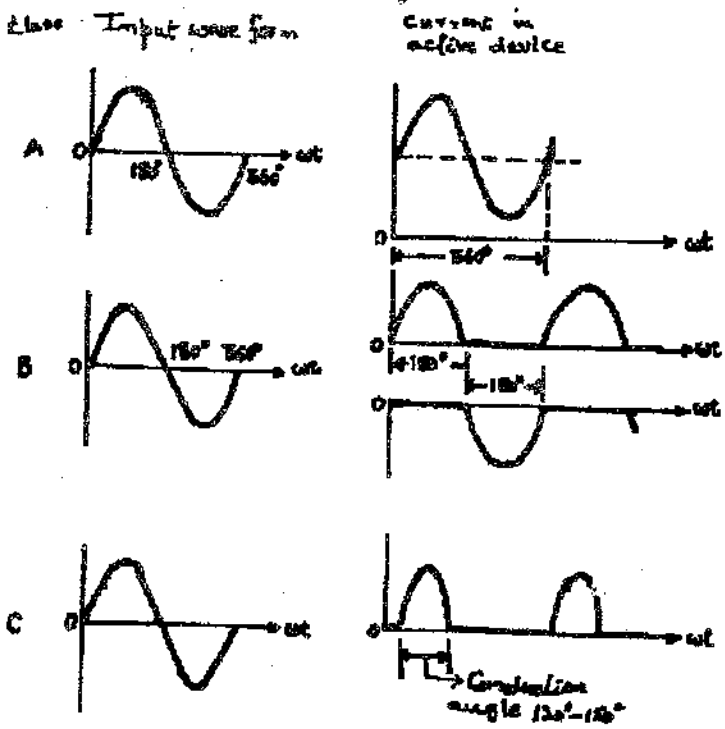


Fig. 6.3 Different cases of Amplifier operations

6.3 AMPLIFIER PARAMETERS

The following are some of the parameters that characterises the behaviour of the amplifier.

(a) Voltage gain (A_V):

The ratio of the output voltage (V_O) to the input voltage (V_i) is called the voltage gain. It can be measured by feeding a signal of a particular frequency to the amplifier and measuring its output voltage as shown in Fig. 6.4.

$$\text{Voltage gain } A_V = \frac{V_o}{V_i} \qquad \ldots (6.1)$$

Fig. 6.4. Experimental set up to measure Amplifier parameters
A= Amplifier; Vs = Signal source

(b) Current gain (A_i):

It is defined as the ratio of the output current (i_O) to the input current (I_i). It can be measured by feeding a known current i_i and measuring the output current using the set-up shown in Fig. 6.4.

$$\text{Current gain } Ai = \frac{i_o}{i_i} \qquad \ldots (6.2)$$

$$\text{The normalized gain} = \frac{A}{A_{max}} \qquad \ldots. (6.3)$$

$$I_i = \frac{V_S - V_i}{R} \text{ and } V_O/R_L$$

$$A_i = \left(\frac{V_O}{V_S - V_i}\right)\left(\frac{R}{R_L}\right) \qquad \ldots(6.4)$$

(c) Power gain (Ap): The product of A_V/A_i is cal led the power gain. The output power is given by

$$P_{out} = V_O^2/R_L \qquad \ldots(6.5)$$

(d) Input resistance (R_i): It is the resistance looking into the input terminals; $R_i = V_i/I_i$. It can be measured using the set-up shown in Fig. 6.4 R is varied until half the source voltage V is obtained at the input terminals.

$$Ri = \frac{V_i\ R}{V_S - V_i}\ R_L \qquad \ldots(6.6)$$

(e) Output resistance (R): It is defined as the resistance seen by a generator connected in the amplifier output when the source resistance is connected across the input terminals. It can be measured by feeding the amplifier shown in Fig. 6.4 by signal, say at 1 KHz and measuring the output voltage with R_L connected across the output terminals (V_O) and R_L disconnected (V_∞).

$$R_O = \frac{V_{ce} - V_O}{V_O} R_L \qquad \ldots(6.7)$$

In the former case, the output voltage is where , $V_O = I_O \dfrac{R_O\ R_L}{R_O + R_L}$ where I_O is the output current. The output impedance is the parallel combination of R_O&R_L. In the latter case, in order open circuit conditions of the output terminals, the output voltage $V_{OC} = R_O I_O$. From these two relations we get $R_0 = \dfrac{V_{ce} - V_O}{V_O} R_L$ (t)

Efficiency (n): As mentioned earlier, the power amplifier converts DC power into signal power. The efficiency of the amplifier for this conversion is given by

$$\eta = \frac{RMS \text{ Value of Signal Power}}{DC \text{ Power}} \qquad \ldots(6.8)$$

(g) Frequency response: The frequency response of a typical amplifier is shown in Fig. 6.5. The gain of the amplifier is constant over a fixed frequency range. It is called the mid frequency range. Let the gain in the range be A. The gain falls off at lower and higher frequencies. The frequency where A drops to 0.707 of mid-frequency gain is indicated by f_L on the low frequency side. It is known as on the high frequency side. f_L and f_H are called lower and upper half- power frequencies.

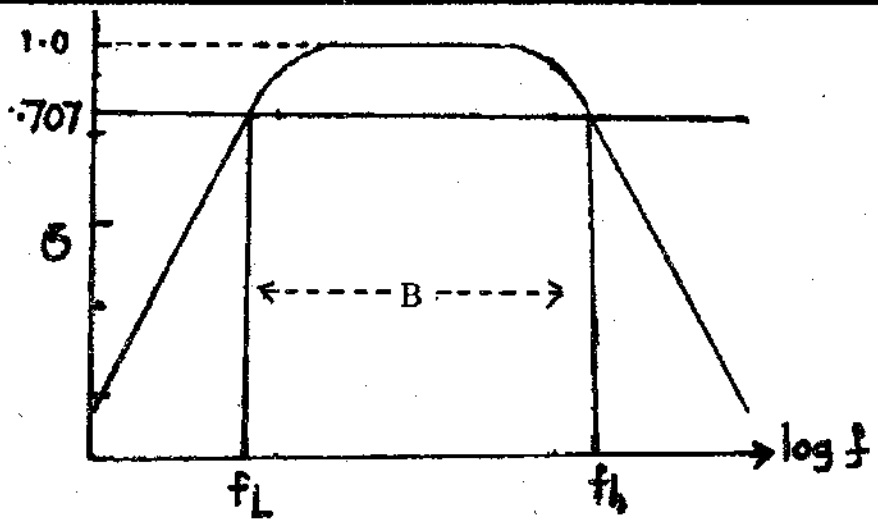


Fig. 6.5. Frequency response of an amplifier G = Gain;
f_L, f_H = half Power Point

The bandwidth is defined as

$$B = (f_H - f_L) \qquad ...(6.9)$$

Power is proportional to the square of the voltage. Hence when A drops to 0.707 of its mid frequency value, power drops to half of its mid-frequency value. Hence f_L and f_H are also called half-power points. They are also called 3 dB points.

6.4 SUMMARY

Amplifiers may be classified in a variety of ways, based on the method of analysis, frequency, method of coupling, angle of flow of the output current. Gain (Voltage Current and power). Input resistance, output resistance, Efficiency and frequency response are important parameters of different amplifiers.

6.5 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail

1. Discuss different methods of classifying amplifiers.

2. What are the parameters that describe the performance of an amplifier. How do you measure the following parameters? Voltage gain, Current gain, input impedance and output impedance.

II. Answer the following questions briefly.

1. What is a transfer function? How do you classify amplifiers based on the transfer function?

2. Distinguish between class A,D,C amplifiers.

III. Solve the following problems.

1 The AC output power of an amplifier is 0.1 Watt. The Vee = 20V and Ie = 20 mA Calculate the efficiency. [Ans: 25%] (Hint: Input DC Power is Vee Ie)

2. The lower and uppercut off frequencies of an amplifier are 100 Hz. and 10 KHz. What is its bandwidth? (Ans: 9.9 KHz)

6.6 References

1. Electronic Devices & Circuits	Jocob Millman and C.C. Halkias
2. Integrated Electronics	Jocob Millman and C.C. Halkias
3. Electronic Devices & Circuits	David A. Bell
4. Electronic Circuits	Schilling Donald
5. Integrated Circuits	K.R. Bothkar
6. Basic Electronics	Grob and Bernard
7. Electronic Principles	Malvino Albert

Contents:

7.0 AIMS AND OBJECTIVES

This unit introduces you to the principle of working of the common emitter amplifier.

After going through this unit you can arrive at the equivalent circuit of the CE amplifier for the evaluation of its parameters and arrive at the expressions fo the gain (Voltage & current) input resistance and output resistance.

7.1 INTRODUCTION

Transistor amplifier circuits are classified according to which element of the device is common to the input and output circuits. The three possible configurations are: Common-Emitter (CE) Common Base (CB) and Common-Collector (CC) amplifiers. Common-Emitter amplifier is the most popular configuration. As such this configuration is analysed in this unit.

7.2 SINGLE - STAGE BJT AMPLIFIER

A single common-emitter amplifier is shown in Fig. 7.1. Resistors R_1, R_2, R_E and R_L are bias resistors needed to set up an appropriate operating point. Capacitors Ct and Cz are called coupling capacitors. They block the direct current i.e., they prevent direct current from entering the signal source and the load. The capacitor CD is called the bypass capacitor as it shorts-out RE at signal frequencies.

In order to analyse the small-signal behaviour of the amplifier, the following rules are to be followed:

(a) Draw the actual circuit diagram and mark the points B (Base), C (Collector), and E (the Emitter).

(b) Replace the transistor by its model.

(c) Transfer all components (resistors, capacitors and signal sources) from the actual circuit to the equivalent circuit.

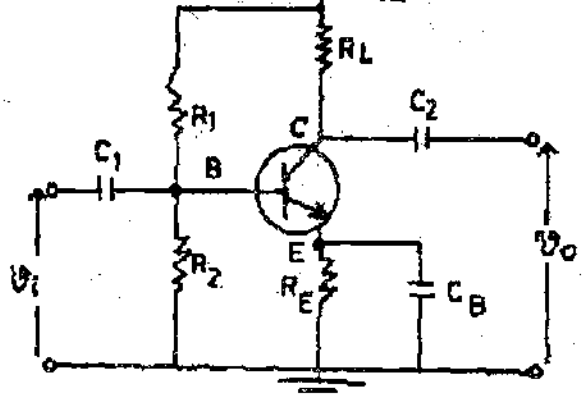


Fig. 7.1. Single stage BJT Amplifier

(d) Since we are interested only in changes from the Q-point, replace each independent dc source by its internal resistance. The ideal voltage source is replaced by a short circuit, and the ideal current source by an open circuit.

(e) Analyse the resulting linear circuit by applying Kirchoff's rules.

The above procedure is valid for any configuration. The only limitation is that the voltages and currents should be small enough so that linear operation results.

7.3 TWO-PORT REPRESENTATION OF A TRANSISTOR

A transistor has two ports i.e., two pairs of terminals. The signal is applied to the input pair of terminals (called the input port). The output is taken from the output pair of terminals (called the output port), as shown in Fig. 7.2. The behaviour of such two port devices is specified by four variables two-signal currents i_1, and i_2 and two signal voltages V_1 and V_2.

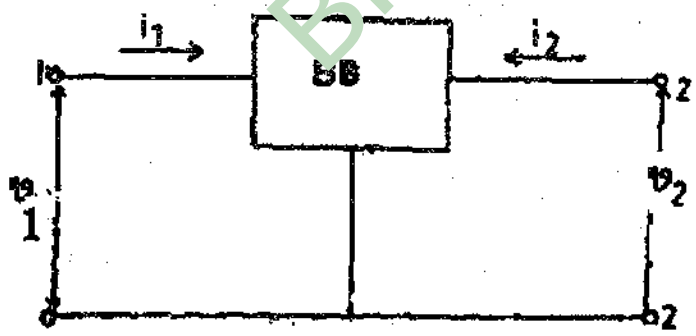


Fig. 7.2. Two-Port Representation of a Transistor
BB=Black box, 11 = input port 22= output part

Any two of them may be taken as independent variables and the other two as dependent ones. This leads to several pairs of equations that describe the behaviour of the transistor.

Treating the input current i_1, and the output voltage V_2 as independent variables, we may write

$$V_1 = h_{11} i_1 + h_{12} V_2 \qquad ...(7.1)$$

and

$$i_1 = h_{21} i_1 + h_{22} V_2 \qquad ...(7.2)$$

Here

$h_{11} = \frac{V_1}{i_1}\Big|V_2 = 0$ = input impedance when the output is short-circuited to ac.

$h_{12} = \frac{V_1}{V_2}\Big|V_2 = 0$ = reverse voltage amplification factor when the input is open circuited to ac.

$h_{21} = \frac{i_2}{i_1}\Big|V_2 = 0$ current gain when the output is short-circuited to ac,

and

$h_{22} = \frac{i_2}{V_2}\Big|i_2 = 0$ = output admittance when the input is open-circuited to ac.

As h_{11}, h_{12}, h_{21} and h_{22} have different dimensions, they are called the h or hybrid parameters.

The equivalent circuit of the transistor in terms of the h-parameters is shown in Fig. 7.3.

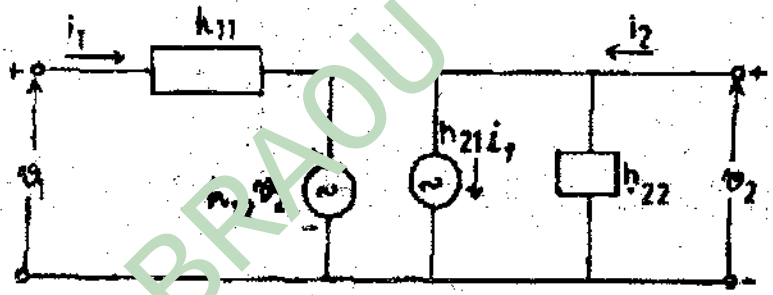


Fig. 7.3 h-parameter equivalent circuit of a transistor

The commonly used notation for the h-parameters are: $h_{11} = h_i$; $h_{12} = h_r$; $h_{21} = h_f$ and $h_{22} = h_o$ The 'i' in h_i stands for the input and the 'r' in h_r represents reverse, the f in h_f represents the forward and 0 in h_O re presents output. For the CE configuration, h_i is written as h_{ie}, h_r as h_{re} h_f as h_{fe} and h_O as h_{Oe}.

7.4 APPROXIMATE SMALL-SIGNAL MODEL OF BJT

A simple but useful small-signal model of the BJT at low frequencies is shown in Fig. 7.4. In this model, we have neglected the presence of the reverse voltage source h_{12} V_2 or h_{re} V2 and the output admittance h_{22} of h_{oe}. For the CE configuration the values of these parameters are $h_{ie} = 12X10^{-4}$ and $h_{oe} = 40X10^{-6}$ mhos.

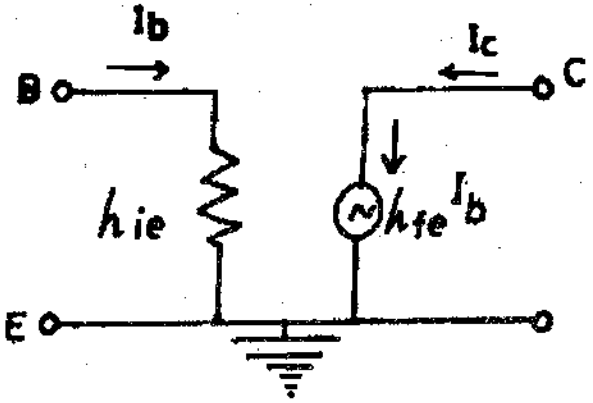


Fig. 7.4. Approximate model for the transistor

These values may safely be neglected. It is not going to affect the conclusions very much.

7.5 PARAMETERS OF CE AMPLIFIER

The common-emitter amplifier shown in Fig. 7.1 gets reduced to the one shown in Fig. 7.5a, if we omit the biasing resistors, coupling and bypass capacitors. There will be a particular frequency range over which these components do not affect the response of the amplifier, we designate that range as the mid-frequency range.

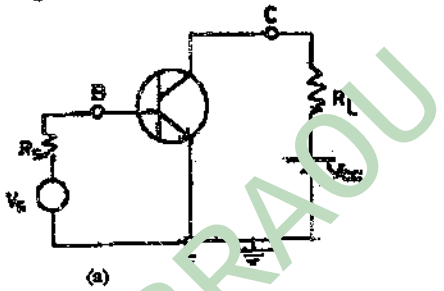
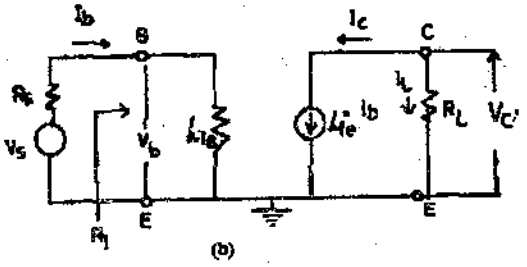


Fig. 7.5 (a) CE, amplifier simplified circuit (Equivalence circuit approximate model)

On either side of this mid frequency range, the gain falls off due to capacitive effects. The effect of these capacitors be discussed subsequently.

Fig 7.5b shows the CE amplifier with the transistor replaced by the approximate



model shown in Fig. 7.4. The voltage gain, current gain, the input resistance, and the output resistance may be evaluated using the equivalent circuit shown in Fig. 7.5b.

(a) Current Gain (A_i):

$$A_i = \frac{I_L}{I_b} = -\frac{I_C}{I_b}$$

But $I_C = h_{fe} I_b$

$$\therefore A_i = -h_{fe} \qquad ...(7.3)$$

(b) Input Resistance (R_i): The resistance R in Fig. 7.5 represents the signal-source resistance. The resistance we see by looking into the transistor input terminals B and E is the amplifier. Input resistance R_i or

$$R_i = \frac{V_b}{I_b} = h_{ie} \qquad ...(7.4)$$

(c) Voltage Gain (A_V): the ratio of the output voltage V_C to input voltage V_b gives A_V.

$$A_V = \frac{V_C}{V_b} = \frac{I_L R_L}{I_b \; h_{ie}}$$

$$= A_i \frac{R_L}{R_i} \qquad ...(7.5)$$

$$= -\frac{h_{fe} R_L}{R_i} = -\frac{h_{fe} R_L}{h_{ie}} \qquad ...(7.6)$$

(d) Output Resistance (R_O): By definition the output resistance R_O is obtained by setting the source voltage V_B to zero and load resistance R_L to infinity and by driving the output terminals from a generator V_2. If the current drawn from V_2 is I_2, then

$$R_O = \frac{V_2}{I_2} \text{ with } V_B = 0 \text{ and } R_L = \infty \qquad ...(7.7)$$

with $V_S = 0$ in Fig 7.5 the input current I_b is zero.

Hence $I_2 = I_C = h_{fe}. \; I_b = 0$

$$R = \frac{V_2}{0} = \infty$$

The CE amplifier, using the simple h-parameter model, has infinite output resistance. If we take the load resistance into consideration it is simple R_L.

7.6 FREQUENCY RESPONSE OF CE AMPLIFIER:

For an amplifier stage, the frequency characteristics may be divided into three regions: There is a range of frequency called the mid-band frequencies, over which the gain is constant. The characteristics obtained in section 7.5 ignoring the capacitances belong to this midband classification. For purposes of discussion let the midband gain be unity (A = 1). In the second (low-frequency) region, the coupling capacitors play an important role in decreasing the gain. In this range, the input signal (V_B) is given to the potential division network consisting the blocking capacitor and the input resistance of the amplifier as shown in Fig. 7.7. As the frequency is decreased from the mid-frequency range, the capacitive reactance goes on increasing. As a consequence more and more voltage is dropped across the blocking capacitor.

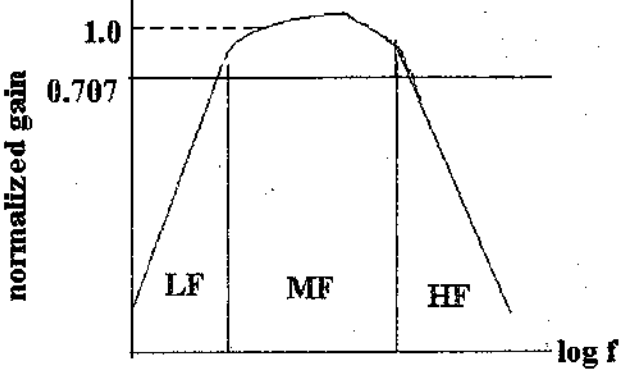


Fig.7.6 Frequency response of CE amplifier
LF = Low Frequency Region
MF = Mild Frequency Region
HF = High Frequency Region

This makes the signal available to the amplifier (V_i) less and less. It approaches, zero at dc.

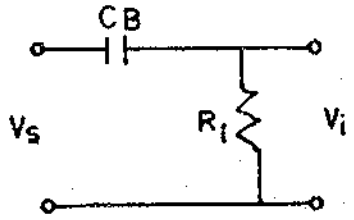


Fig. 7.7 Decrease of gain at low frequencies

In the third (high-frequency) region, above mid band, shunt capacitors within the device or due to wiring playa prominent role in determining the frequency response. The circuit then behaves as a low-pass filter shown in Fig. 7.8. The output voltage of the amplifier feeds this filter. As the frequency increases, the capacitive reactance decreases making the output less and less. Finally it becomes zero at very high frequencies. The total frequency response is shown in Fig. 7.6.

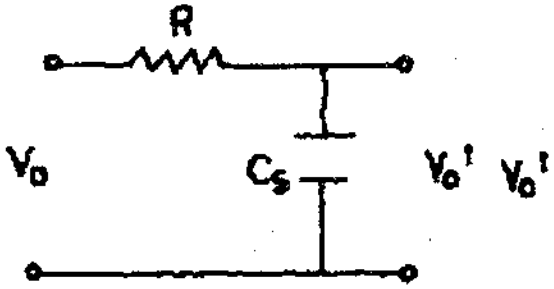


Fig. 7.8 Decrease of gain at high frequencies

7.7 SUMMARY

Out of three possible configurations for the transistor amplifier, the most common configuration is CE amplifier. Applying Krichoff's laws to the equivalent circuit of the amplifier expressions for its parameters hybrid or –h can be arrived.

7.8 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the Circuit diagram of a CE amplifier and explain its working. Draw its

equivalent circuit and arrive at its characteristic parameters.

II. Answer the following questions briefly.

1. Discuss the role of BJT as an amplifier:
2. Discuss the frequency response of a CE amplifier.
3. Draw the equivalent circuit diagram common emitter amplifier.
4. What are h-parameters? Discuss.

7.9 References

1.	Electronic Devices & Circuits	Jocob Millman and C.C. Halkias
2.	Integrated Electronics	Jocob Millman and C.C. Halkias
3.	Electronic Devices & Circuits	David A. Bell
4.	Electronic Circuits	Schilling Donald
5.	Integrated Circuits	K.R. Bothkar

UNIT 8: NEGATIVE FEEDBACK IN AMPLIFIERS

Contents:

8.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

1. Feed back in Amplifiers
2. Types of feedback
3. Emitter follower

After going through this unit you can examine the effect of negative feedback on amplifier performance, advantages of negative feedback over positive feedback and derive the expressions for the parameters of emitter follower.

8.1 INTRODUCTION

A part of the output of an amplifier may be fed back to stabilize its performance. Through intentional use of feedback, the gain of the amplifier can be made much greater or more stable or less sensitive to change. In this unit, we study the basic concept of feedback and the general benefits of negative feedback.

8.2 GAIN OF AN AMPLIFIER WITH NEGATIVE FEEDBACK

The block diagram of feedback amplifier is shown in Fig 8.1.

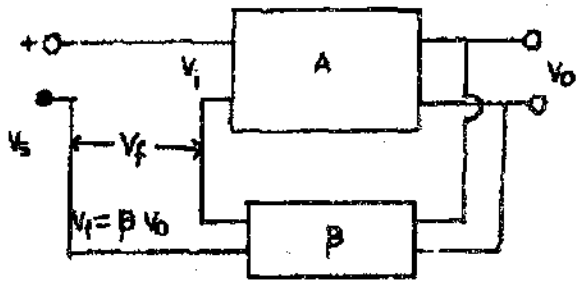


Fig. 8.1 Principle of Feed back Amplifier A = Amplifier of gain A and β = Feedback ratio or Feedback Factor

The symbol A represents the ratio of the output voltage V_O to the input voltage Vi. It is the gain of the amplifier without feedback. It is also called the open-loop gain. The block containing β represents an arrangement for tapping off a portion V_f of the output voltage V_O and feeds it back into the input in phase opposition to the input signal, thus closing the loop. The feedback factor

$$\beta = \frac{V_f}{V_o} \qquad \text{or} \qquad V_f = \beta\ V_O \qquad \ldots(8.1)$$

In general β is a complex quantity if reactive elements like inductors and capacitors are used. It is a real number if we only use pure resistive elements in the feedback network. The Feedback Voltage may be proportional to the output voltage or output current. The former is called voltage feedback while the latter is called the current feedback.

A fraction of the output is fed back in series with the signal voltage V_S then the resultant input to the amplifier is given by

$$V_i = V_S - V_f \qquad \ldots(8.2)$$

The output voltage is now given by

$$V_O = A_O V_i = A_O (V_S - V_f) = (A_O V_S - A_O V_f)$$
$$V_O = A_O V_S + A_O \beta V_O$$

Rearranging, we get

$$V_O (1 + \beta\ A_O) = A_O V_S$$

Or

$$A_f = \frac{V_O}{V_S} = \frac{A_O}{1 + \beta A_O} \qquad \ldots(8.3)$$

where A_f is the gain with feedback. Eqn (8.3) is the basic equation that reveals the performance of the feedback amplifier with feedback. In general A, and (βA_O) are complex numbers.

Even though the gain decreases, with negative feedback, it offers several other advantages. They are discussed in the next section.

8.3 EFFECTS OF NEGATIVE FEEDBACK

(a) **Gain Stabilization:** The gain of an amplifier with negative feedback is given by

$$A_f = \frac{A}{1 - \beta\ A}$$

If $|\beta\ A| >> 1$, we can neglect 1 in the denominator in comparison of βA_O then

$$|A_f| = -\left|\frac{1}{\beta}\right| \qquad \ldots(8.4)$$

Thus A_f is independent of the open-loop gain A of the amplifier. It depends only on the feedback ratio, which in term depends upon the elements of the feedback network. If the feedback network consists of only resistors, it is independent of frequency. The open-loop gain of the amplifier A depends on the supply voltage variations, aging and temperature variations. However, they do not affect the gain of the amplifier A_f with negative feedback. Thus negative feedback stabilizes the gain of the amplifier A_f.

(b) Reduction of Distortion: When the amplifier is fed by a large amplitude signal, the output signal is distroted. The output voltage including distortion is then given by

$$Vo = AV_i + D \qquad \ldots(8.5)$$

where D is the distortion voltage. With negative feedback,

$$V_{Of} = \frac{AVi}{1+\beta A} + \frac{D}{1+\beta A} \qquad ...(8.6)$$

Negative feedback reduces distortion by a factor (1 + β A). The signal also decreases by the same extent. But this reduction can be compensated by increasing the input signal level. The output voltage without negative.

(c) Noise Reduction: The output voltage without negative feedback, including noise is give by

$$V_O = AV_i + N \qquad ...(8.7)$$

the noise (the wanted signals) appearing at the input terminals of an amplifiers are naturally amplified along with the input signals. The negative feedback reduces the noise also by factor (1 + β A).

$$V_{OF} = \frac{AVi + N}{1+\beta A} = \frac{AV_i}{1+\beta A} + \frac{N}{1+\beta A} \qquad ...(8.8)$$

(d) Improvement of Bandwidth: According to Equ. (8.4), the gain is independent of frequency i.e., it has infinite bandwidth. However, at low and high frequencies the condition we assumed in arriving at Equ. (8.4) i.e., | β A | >> 1 does not hold good. This is due to the fact that A decreases. Hence the gain of the amplifier with feedback also decreases at low and high frequencies. However, the bandwidth will be larger than the bandwidth with negative feedback of the amplifier, without feedback as constant in fig 8.2. Since the gain bandwidth product for an amplifier is constant

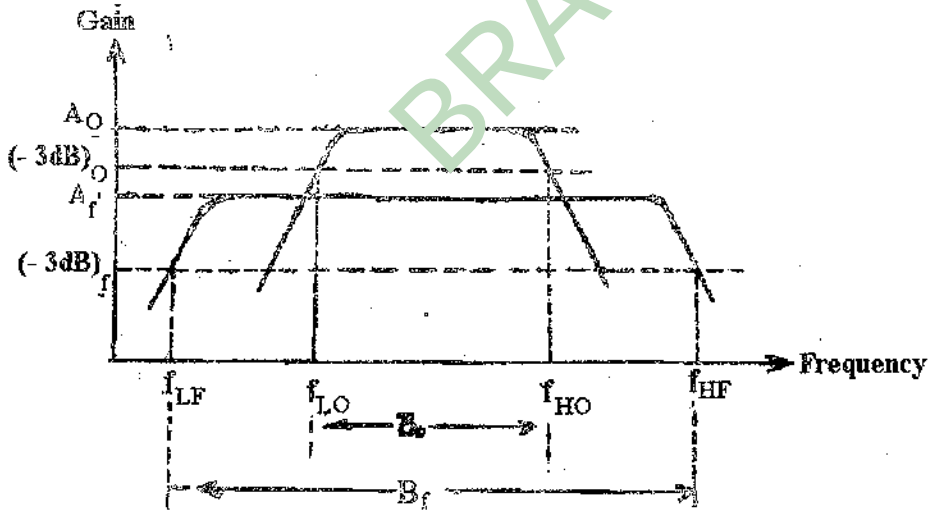


Fig 8.2. Frequency response of an amplifier without and with Negative feedback

$$A.B = A_f . B_f \qquad ...(8.9)$$

Since A_f decreases with negative feedback, B_f increases by a factor (1 + β A).

(e) Effect on Input and Output Impedances: Negative feedback modifies the input and output impedances of an amplifier. The input impedance may decrease or increase depending upon how the feedback signals are combined with the input signal. However, it is independent of how the feedback signal is obtained from the output.

Similarly, the output impedance may also increase or decrease depending on the way of obtaining the feedback signal from the output. It does not depend on the way in which the feedback signal is combined with the input signal.

8.4 EMITTER FOLLWER OR COMMON COLLECTOR AMLIFIER

A practically useful form of feedback amplifier is emitter follower shown in fig 8.2. It is a special case of voltage series feedback arrangement.

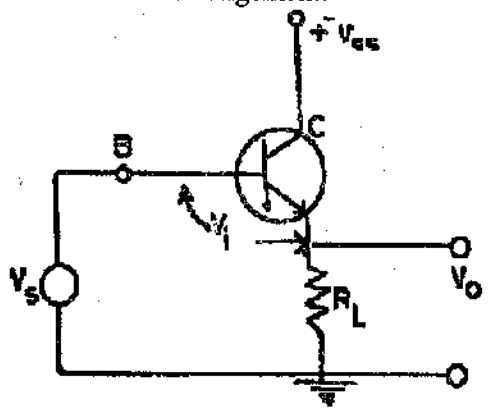


Fig. 8.3 Emitter Follower

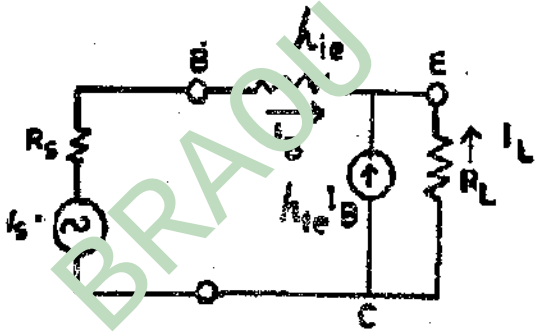


Fig. 8.4 Emitter Follower Equivalent circuit

Here the voltage V_O is developed across the load resistance R_L connected to the emitter. The entire output voltage V_O is feedback in series with the input signal V_S. Thus the voltage fed back (V_f) is equal to the output voltage V_O. Hence $\beta = 1$. It may also be noted that the effective input signal applied to the transistor (V_i) is equal to the difference between the externally applied voltage (V_S) and the output voltage V_O i.e. $Vi = V_S - V_O = V_B - V_f$. Hence the feedback is negative.

The parameters of this configuration can be evaluated using the approximate model discussed previously. The approximate equivalent circuit of the emitter follower is shown in Fig. 8.4. Examination of the equivalent circuit leads to the following expressions:

(a) Current gain: From Fig. 8.4, we see that

$$A_i = \frac{-I_e}{I_b} = \frac{(1+h_{fe})I_b}{I_b} = 1 + h_{fe} \qquad ...(8.10)$$

(b) Input resistance (Ri): From Fig. 8.3, we obtain

$$R_i = \frac{V_b}{I_b} = \frac{\left[h_{fe} + (1+h_{fe})R_L\right]I_b}{Ib} \qquad ...(8.11)$$

$$= h_{ie} + (1+h_{fe})R_L$$

$\approx h_{ie} + A_i R_L$

(c) Voltage gain (A_V): The voltage gain is related to the current gain Ai via the relation,

$$A_V = A_i \frac{R_L}{R_i}$$ (Please see Eqn. 7.5)

$$1\text{-}A_V = \frac{Ri - A_i R_L}{R_i}$$

Combining with Eqn (8.8) we get

$$1\text{-}A_V = \frac{h_{fe}}{R_i}$$

or

$$A_V = 1 - \frac{h_{fe}}{R_i} \qquad ...(8.12)$$

(d) Output impedance: In Fig: 8.3, the open circuit voltage is V_S and the short-circuit output current is

$$I = (1 + h_{fe})\, I_b = \frac{(1 + h_{fe})V_S}{h_{ie} + R_s}$$

$$R_O = \frac{V_{ie}}{I} = \frac{R_S + h_{ie}}{1 + h_{fe}}$$

8.5 SUMMARY

Negative feedback in Amplifiers can outweigh the loss in gain the input and output impedances of the amplifiers can be improved. Noise and distortion can be reduced. Emitter follower is an amplifier employing negative feedback, having gain less than unity, high input impedance and low output impedance.

8.6 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the circuit diagram of an emitter follower. Arrive at its equivalent circuit. Calculate the voltage gain, current gain input resistance and output resistance of this amplifier.

II. Answer the following questions in brief.

1. What factors limit the operating region of transistor in power amplifiers?
2. Discuss the concept of feedback. Distinguish between positive and negative feed back.
3. Discuss the effect of negative feedback on amplifier performance.

8.7 REFERENCES

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6.	Basic Electronics	Grob and Bernard
7.	Electronic Principles	Malvino Albert

UNIT 9: POWER AMPLIFIER

Contents:

9.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

1. Power amplifiers,
2. Working of a push pull amplifier

After going through this unit, you can draw load lines for a simple amplifier and a transformer coupled power amplifier to the operating point. You can derive an expression for the theoretical efficiency of a class-A amplifier.

9.1 INTRODUCTION

To drive the loudspeaker in a public address system requires appreciable amount of power. Amplifiers that can deliver appreciable amount power is called power amplifier. It involves large signals, which do not confine to the linear portion of the device characteristics. As such the resulting non-linear effects have to be taken into account, power amplifiers have to provide the required power output with a stable circuit and use the transistor efficiently and safely.

9.2 OPERATING REGION

An amplifier has to provide power to its load without exceeding the voltage, current and power rating limitations of the device. The permissible operating region of a particular transistor is indicated on its characteristics as shown in Fig. 9.1. Curve A represents the maximum allowable power dissipation P_D of the transistor, it is a hyperbola defined by

$$V_{CE} I_C = P_C - P_O \qquad \ldots(9.1)$$

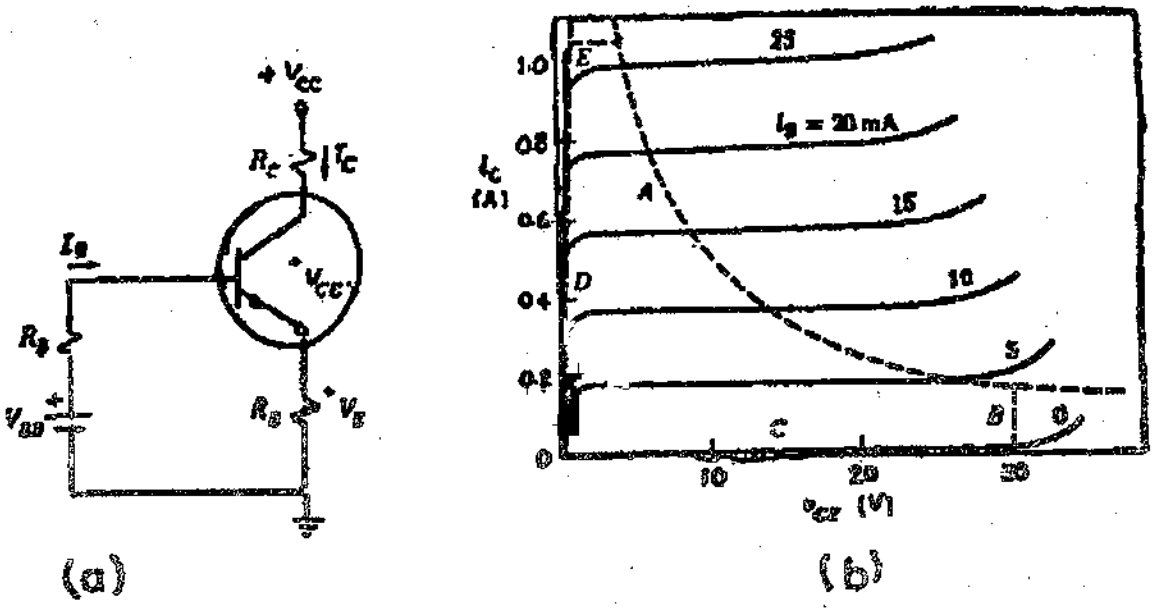

Fig 9.1 Permissible operating region of a transistor
(a) circuit (b) characteristics

Where P_D is established by the manufacturer. Operation above this line may damage the device. Line B represents the fact that higher collector voltages lead to non-linear effects. Line C bounds the region in which the collector current is approaching zero i.e., the collector goes into cut-off. Line D bounds the saturation region in which a further increase in the signal does not produce a corresponding increase in the output current. Line E represents a limit within which the manufacturer guarantees its specifications.

9.3 FIXING THE QUISCENT OPERATING POINT - Q

The bias arrangement locates and maintains' operation in the permissible region. Subject o these limitation, we would like to extract maximum power output. In general, the load line should lie just below the maximum dissipation curve. Its slope should reflect a compromise between large signal and low distortion.

The factors influencing the choice of Q point and load resistance are shown in Fig. 9.2, where RL is assumed to be in the collector circuit. Point Q_1 is well below the maximum dissipation curve and does not permit maximum voltage and current swings. A second possibility is Q_2 where the load line $R_{L2} < R_{L1}$ is drawn tangent to the hyperbola; this permits same voltage swing as Q, and larger Current swing. The load line for $R_{L3} > R_{L1}$ permits the same current swing as Q_1, and a larger voltage swing.

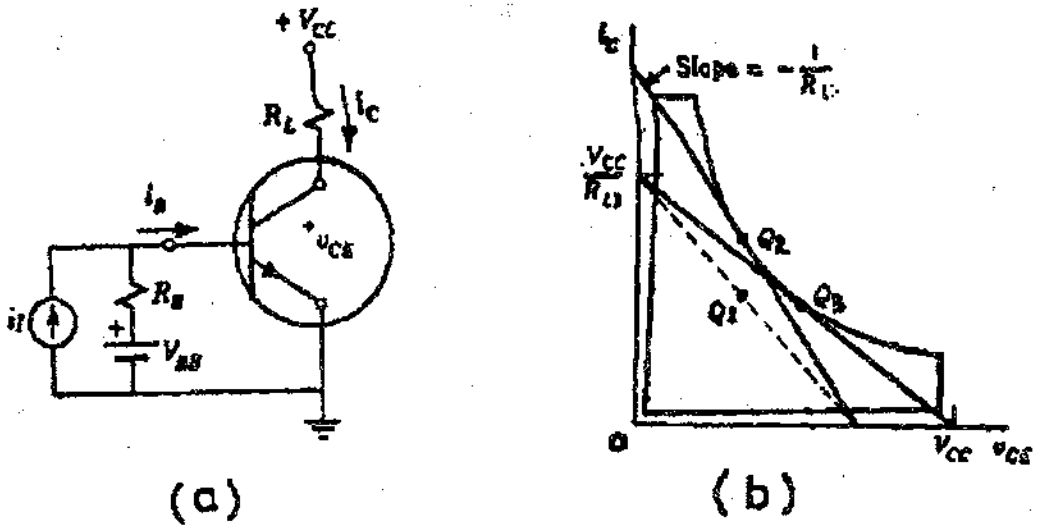

Fig. 9.2 Location of the load line for a simple amplifier
(a) Amplifier Circuit (b) Operating region

Operation at any point along the maximum dissipation curve between Q_2 and Q_3 will permit approximately the same signal power output.

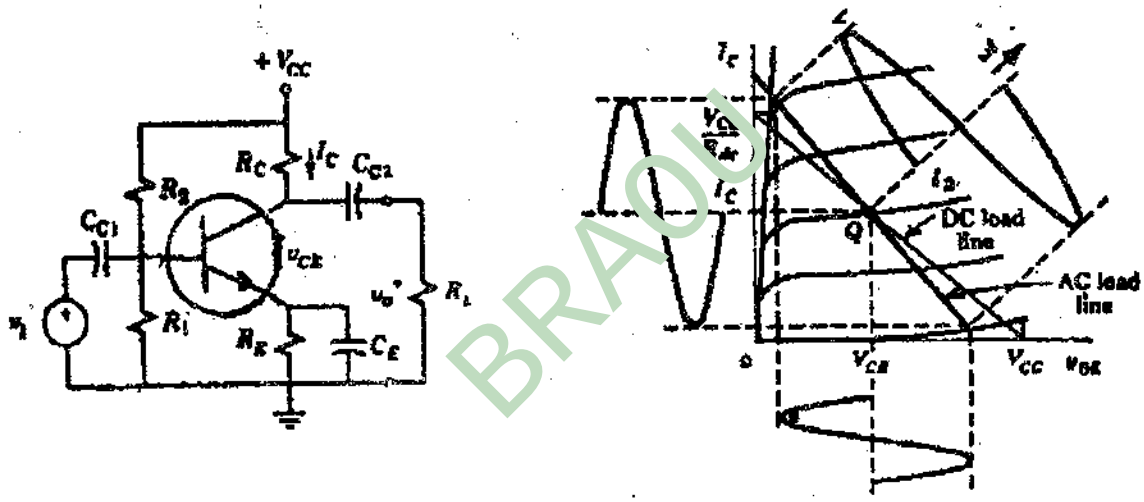

Fig 9.3 Operation of a large-signal amplifier
(a) Amplifier Circuit (b) Load line Construction

Fig 9.3 (a) shows a practical amplifier. It involves some additional factors. The capacitances block dc bias currents. The effective dc load $R_{DC} = R_C + R_B$. For maximum voltage swings, operation-should be near the midpoint of the load line or V_{CC} Ω2V_{CE} Since the quiescent value V_{CE} is given by

$$V_{CE} = V_{CC} - I_C R_{DC} \qquad \ldots(9.2)$$

$$R_{DC} = R_C + R_E \| \frac{V_{CE}}{I_C} \qquad \ldots(9.3)$$

It is typical design condition.

The ac signals see a different circuit. Since $R_B = R_1 R_2$ is made large, most of the signal current flows into the base. CE short-circuits RB at the signal frequency; therefore R_E is effectively removed. V_{CC} is a steady dc source and there won't be any ac voltage across it, therefore the upper end of R_C is effectively grounded for signals. C_{C2} is an ac short-circuit, therefore R_C and R_L are effectively in parallel across V_O. The ac load line is

defined by

$$R_{ac} = R_C \| R_L = \frac{R_C \ R_L}{R_C + R_L} \qquad \ldots(9.4)$$

It is shown in Fig 9.3 b. For this circuit, $R_{dc} > R_{ac}$. The optimum location of the Q point is at the midpoint of the ac load line. What do these ac and dc load lines represent? The ac load line defines the relation between the signal values and the device characteristics. The dc load line just identifies the supply voltage V_{CC} required for operation at Q.

9.4 CLASS A POWER AMPLIFIER WITH DIRECT COUPLED LOAD

The circuit diagram of class – A power amplifier with direct coupled load resistance is shown in Fig. 9.4(a) and the load line and Q-point fixation are shown in Fig.9.4 (a) and (b).

The AC power output from the circuit can be estimated through the load line analysis shown in Fig. 9.4 (b).

$$\text{The AC power output } P_O = \frac{(V_{emax} - V_{emin})}{2\sqrt{2}} \ \frac{(I_{emax} - I_{emin})}{2\sqrt{2}} \qquad \ldots(9.5)$$

Where $V_{emax} = V_{CC}$

$V_{emin} = V_{ce}|_{sat} \approx 0$

$I_{Cmax} = V_{CC} / R_L$

$I_{emin} \approx$ IC cut off ≈ 0

$$\therefore P_O = \frac{V_{CC}}{2\sqrt{2}} \circ \frac{I_{Cmax}}{2\sqrt{2}} \frac{V_{CC}}{2} (V_{CC}/R_L) \qquad \ldots(9.6)$$

$$P_O = \frac{V_{CC}^2}{8R_L} \qquad \ldots(9.7)$$

DC input power $P_{DC} = V_{CC} \cdot I_C = V_{CC} \left(\frac{I_{max}}{2}\right)$

$$= \frac{V_{CC}}{2} \circ \left(\frac{V_{CC}^2}{R_L}\right) \qquad \ldots(9.8)$$

$$\text{i.e.,} \quad P_{DC} = \frac{V_{CC}^2}{2R_L} \qquad \ldots(9.9)$$

Hence, the efficiency of the amplifier is

$$\eta = \frac{P_O}{P_{DC}} = \left(\frac{V_{CC}^2}{8R_L} \Big/ \frac{V_{CC}^2}{2R_L}\right) X100 \qquad \ldots(9.10)$$

$$= (1/4) \text{ X } 100 = 25\%$$

9.5 CLASS – A POWER AMPLIFIER TRANSFORMER COUPLED

In the amplifier circuit shown in Fig. 9.3 a. the supply V cc must exceed the

collector voltage V CE by the voltage drop across the collector resistor R_C I_C. Further, most of the signal power is dissipated in R_C instead of being transferred to R_L. The necessary dc supply voltage can be reduced and the power transfer improved by using a transformer to couple the output signal to the load as shown in Fig. 9.6.

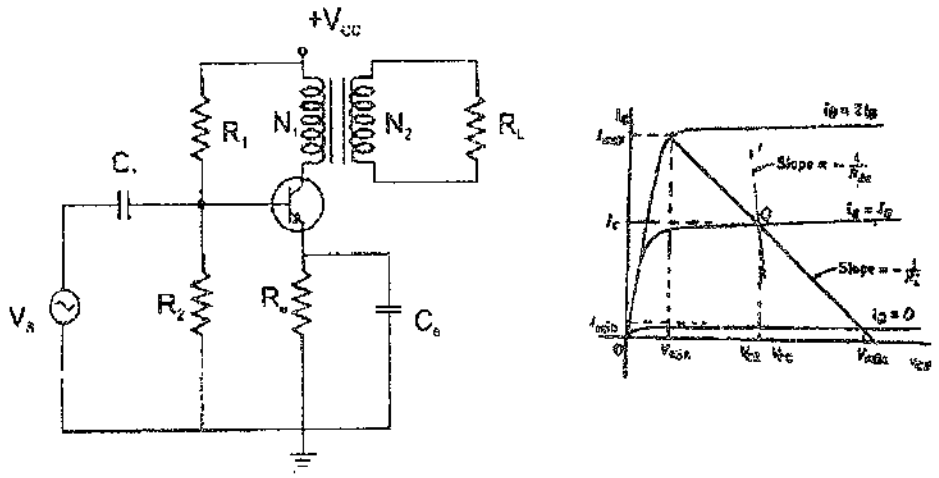

Fig 9.4 Simplified circuit of a transformer-coupled power amplifier
(a) Circuit (b) Load-line

The transformer transfers only ac signals to the load DC currents flow only in the low resistance primary winding. With transformer coupling $V_{CC}=V_{CE}$ instead of $V_{CB} + I_C R_C$ the dc power input is reduced. By proper choice of the turn's ratio, the load impedance can be matched to achieve maximum power transfer. For example, the low impedance of a loudspeaker (R_L cap be made to appear to a transistor as a much higher value (R_L^1) where

$$R_L^1 = \left(\frac{N_1}{N_2}\right)^2 R_L \qquad ...(9.11)$$

$$\left(\frac{N_1}{N_2} = \text{turns ratio}\right)$$

In figure 9.6b, the slope of the ac load line is $\frac{1}{R_L}$. The chosen Q point and the desired signal swing define R_L^1. Once R_L^1 is determined, the turns ratio N_1 / N_2 is selected to provide a match with the actual load resistance R_L. The dc load line has a slope of $-1/R_{dc}$; in this case R_{dc} = Ro + small winding resistance of the transformer primary. Hence $I_C R_{DC} << V_{CE}$ and therefore $V_{CC} \approx V_{CEO}$

Assuming a sinusoidal signal current in a resistive load, the amplit4de of the sinusoid is just one-half of the difference between the maximum and minimum values of current. The rms value is

$$I_C = \frac{I_P}{\sqrt{2}} = \frac{1}{2\sqrt{2}} (I_{max} - I_{min}) \qquad ...(9.12)$$

The output signal power is

$$P_O = I_C^2 R_L^1 = V_C I_C = \frac{V_C^2}{R_L^1} \qquad ...(9.13)$$

Where V_C is the rms value of the signal voltage across R'_L

The dc power supplied by V cc is given by

$$P_{CC} = V_{CC} I_C \ \Omega \ V_{CE} I_C \qquad ...(9.14)$$

The efficiency of the amplifier is given by

$$\text{Efficiency} = \frac{P_O}{P_{CC}} = \frac{V_C I_C}{V_{CE} I_C} \qquad ...(9.15)$$

It may be noted that in the above discussion we assumed class-A operation only.

9.6 EFICIENCY OF THE TRANSFORMER COUPLED CLASS- A POWER AMPLIFIER

The theoretical limit of the efficiency of class-A power amplifier can be determined by considering the ideal amplifier characteristics shown in Fig. 9.5. Signal of amplitude I_B produces a total current swing from $2I_C$ to 0 and total voltage swing from $2V_{CE}$ to zero.

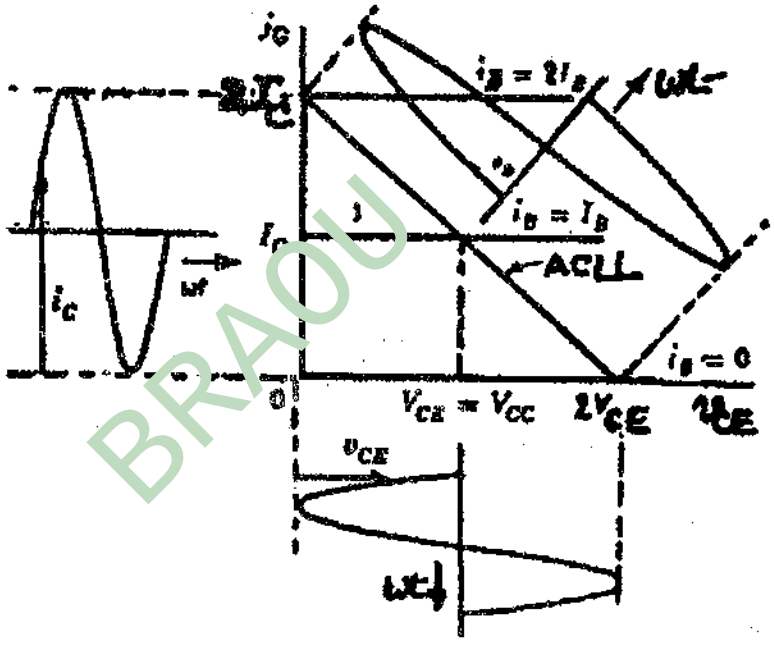

Fig 9.5 Ideal power Amplifier - Operation ACLL= AC Load line

The ideal efficiency is

$$\frac{OutputPower}{InputPower} = \left[\frac{(V_{CE}/\sqrt{2})(I_C/\sqrt{2})}{V_{CE} I_C}\right] X100 = 50\% \qquad ... \quad (9$$

.16)

The theoretical efficiency of 50% is never achieved in practice. This is twice the power component or efficiency of the direct-coupled load.

9.7 PUSH-PULL AMPLIFIERS

The class-A operation discussed above results in low distortion of the output signal. But its efficiency is also low.

If the amplifier is biased to cut-off, output current flows only during the positive half cycle of the input signal and the output is badly distorted. The resulting class-B operation has high efficiency, as the average value of the collector current is low. The distortion can be minimised by using the push-pull arrangement shown in Fig. 9.6. The input transformer receives the signal and applies it to the transistors as shown in the

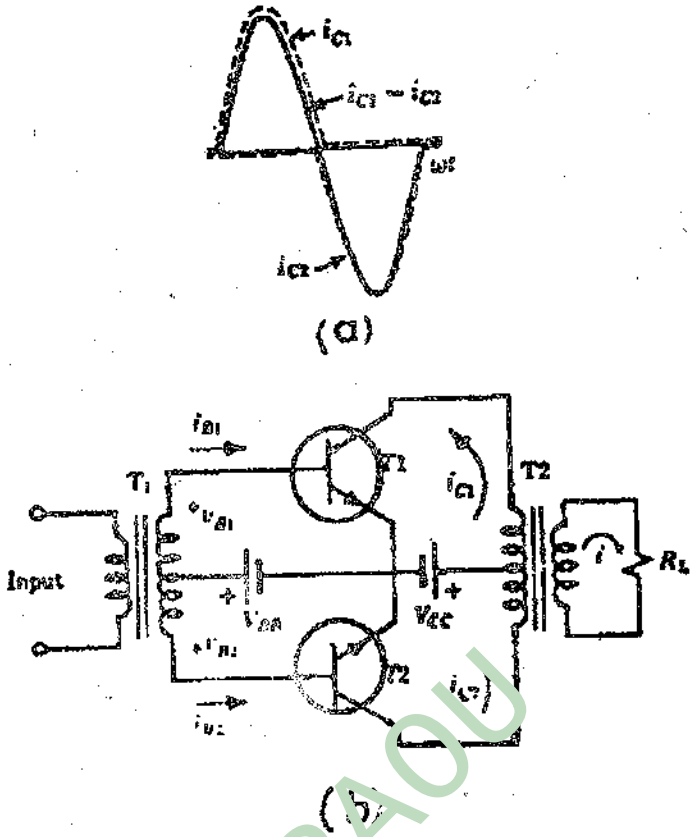

figure.

Fig 9.6 Basic push-pull amplifier circuit
(a) Class-B Operation (b) Circuit diagram

The signals applied to the transistors are out of phase and the resulting collector currents are 1800 out of phase. The output transformer T2 delivers to the load a current that is proportional to the difference of the two collector currents. This reduces the distortion to some extent.

The push-pull amplifier is operated under class-B conditions. Bias supply voltage V_{BB} is set forthemm-on voltage (about 0.7 V for silicon transistors). As V_{B1} goes positive, I_{Bi} begins to flow and I_{Ci} flows (Fig. 9.6 b). Since V_{B2} is negative, transistor T_2 is cut off. When V_{B1} goes negative, V_{B2} is positive and transistor T_2 takes over. If the two transistors have identical characteristics, a nearly pure sinusoidal output results.

The ideal efficiency of a Class-B amplifier can be calculated on the lines similar to the
derivation of eqn (9..8). It works out to 78.5%.

9.7.1 Transformerless class B push pull amplifier

In this method the input transformer is replaced by a phase inverter as shown in figure 9.7. It consists of a NPN transistor with equal R_E & R_C. Emitter output of phase splitter provides in phase signal. The collector output provides out of phase signal. So output signals are equal in amplitude and out of phase.

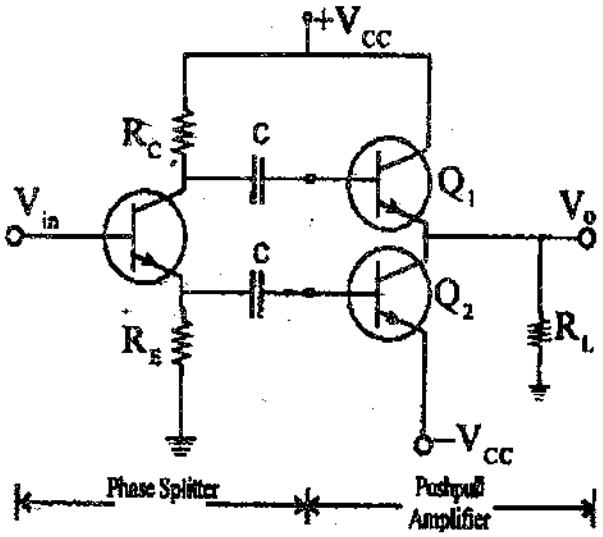

Fig 9.7 Transform less Class B Push Pull Amplifier

The pushpull configuration-using transformer has two major drawbacks namely it requires a bulky and expensive transformer. The second requirement is it necessitates the use of an input transformer to produce the input signal 180^0 out of phase with each other. It makes the circuit more complicated. Thus the transformer less amplifier eliminates both above-mentioned drawbacks. But retaining the advantage of pushpull configuration. Its operation and power relation are identical to the transformer-coupled amplifier. The load is directly connected to the amplifier output because the split supply (i.e., $+V_{CC}$ and $-V_{CC}$) used in the circuit gives an advantage of making the DC component of output power as zero.

9.7.2 Complementary Symmetry Amplifier

In this circuit, the complementary means the circuit uses two identical transistors but one is NPN and the other is PNP. The symmetry means the biasing resistors connected in both transistors are equal. As a result of this emitter base junction of each transistor is biased with the same voltage.

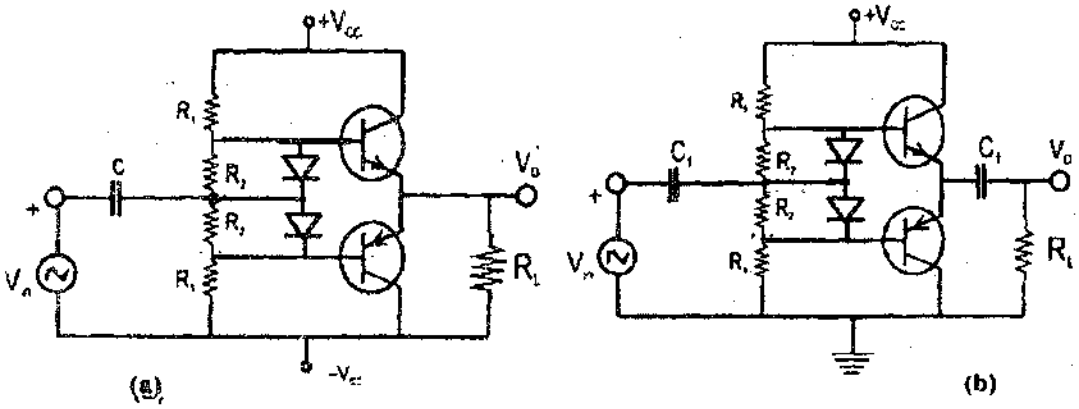

Figure 9.8 Complementary Symmetry Class B Push-Pull Amplifier

When V_i is in the positive half cycle, the base emitter voltage of both transistors becomes positive. To this condition, only the NPN transistor conducts, while the PNP transistor is cutoff. During this process positive half cycle current flow through R_L.

When V_i is in the negative half cycle, only the PNP transistor conducts and the negative half cycle current flows through R_L. Therefore when the output is tapped across

R_L we get a full cycle amplified waveform of the input signal.

It may be noted that the amplifier circuit has a unity gain because of the emitter follower configuration is used. The split supply used in the circuit (Figure 9.8(a)) gives us an advantage that the DC component of output voltage can be made to zero. Thus only ac component of the power is available at the output hence no need of coupling capacitor at the output.

The main disadvantage of this circuit is that the need to use two power supplies However we can realize another complementary symmetry using only one power supply shown in figure 9.8(b). In this figure 9.8(b) when V_1 is positive Q_1 is ON and Q2 is OFF during this process, current flows through T_1, C and R_L thereby charging the capacitor 'C'.

When V_1 goes negative Q_2 is ON and Q_1 is OFF and current flows through Q_2 from the capacitor 'C' which acts as supply. The rest of the operation is similar to that given for the circuit of figure 9.8(a).

Two Diodes of the same material as a transistors used for complimentary symmetry amplifier are included in between the two bases to compensate for the bias asymmetry ($+V_{BE}$ for npn and $-V_{BE}$ for pnp) between the pnp and npn transistors.

9.8 SUMMARY

The operating region of a transistor for power amplification is defined by the maximum allowable current, voltage, power and distortion. Transformer coupling isolates the signal output permits impedance matching and improves efficiency. The push pull amplifier reduces distortion and improves efficiency.

9.9 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the circuit diagram of a transformer-coupled amplifier and discuss its working.

II. Answer the following questions briefly.

1. What is the theoretical limit of the efficiency of a class-A power amplifier? Discuss
2. What is a push pull amplifier? Give its circuit diagram and explain its working.
3. Discuss the operation of an ideal power amplifier.

III. Solve the following problems

1. The AC output power of an amplifier is 0.1 watt. The V_{CC}=20V and I_C = 20 mA. Calculate the efficiency [Ans: 25%] (Hint: Input DC power is Vee Ie)
2. The lower and upper cut-off frequencies of an amplifier are 100 HZ, and 10 kHZ. What is its bandwidth?[Ans : 9.9 KHZ]
3. A fixed-bias circuit uses a transistor with Ω = 0.95. Calculate its stability factor.

[Ans : 20]

4. In a transistor amplifier, the base-emitter voltage varies by 50 m V. This leads to a change of 5V in the output voltage. Calculate the voltage gain.

[Ans : 100]

5. A common-emitter amplifier uses a transistor with hfe =50 and hie =2500 ohms. It uses a load resistance of 5000 ohms. Calculate its voltage gain and output resistance.

[A_V = 100; R_O = 5000 ohms]

6. The h_{fe} of a transistor used in a CE configuration is 80. What is the maximum current gain of the amplifier?

[Ans: 80]

7. The gain of an amplifier without-feedback is 1000. Negative feedback with p = 0.01 calculate the gain with feedback [Use equation 8.3] [Ans: $11\frac{1}{9}$]

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BLOCK – III

OPERATIONAL AMPLIFIERS

UNIT-10: DIFFERENCE AMPLIFIER

Contents

10.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

1) Difference Amplifier

2) Common Mode Rejection Ratio (CMRR)

After going through this unit you will be able to explain the operation of a difference amplifier its characteristics, and its electronic circuit.

10.1 INTRODUCTION

One of the useful and popular amplifier configurations is the difference (or differential) amplifier. It is a direct-coupled amplifier.

It accepts two input signals. The output voltage is proportional to the difference between the two input signals. It rejects signals common to both the inputs (for example- Noise) Hence it is not sensitive to environmental changes. It has many applications in instrumentation. It is the primary input circuit in many linear integrated circuits.

10.2 BASIC DIFFERENCE AMPLIFIER

The basic difference amplifier circuit is shown in Fig. 10.1. It has two identical transistors (T_1 and T_2) with identical resistors in their collector circuits. The two halves of the circuit are perfectly matched. The emitters connected to ($-V_{EE}$) via the emitter resistor R_E properly bias the two transistors. The circuit is energised by a symmetrical power supply (+15V) – 0 – (- 15V).

The emitter resistor R_E is the heart of the difference amplifier. It limits the current available to the two transistors to a constant value I_O. The sum of the emitter currents I_{E1} and I_{E2} is always equal to I_O. Thus R_E - V_{EE} combination acts as a constant current source

Let us now try to understand the working of this amplifier. It has two input terminals

(1 and 2). The output voltage is measured across the two collectors as shown in the figure. Let two voltages of equal magnitude and of the same polarity be applied one between terminal 1 and ground and the other between terminal 2 and ground. This causes equal changes in the collector currents and the potential difference between the two collectors will be zero. This means the voltages common to both the terminals do not affect the output voltage.

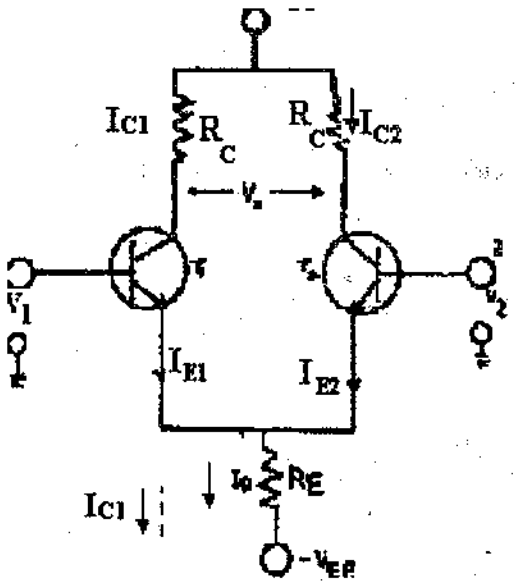

Fig. 10.1: Basic differential Amplifier

Let us now try to understand the working of this amplifier. It has two input terminals (1 and 2). The output voltage is measured across the two collectors as shown in the figure. Let two voltages of equal magnitude and of the same polarity be applied one between terminal 1 and ground and the other between terminal 2 and ground. This causes equal changes in the collector currents and the potential difference between the two collectors will be zero. This means the voltages common to both the terminals do not affect the output voltage.

If the base of Transistor T_1 is driven positive with respect to the base of Transistor T_2 the current through Transistor T_1 increases and the current through Transistor T_2 decreases by an equal amount so that I_O remains constant. Since $I_{C1} > I_{C2}$ a potential difference develops between the two collectors i.e. a differential input voltage causes a differential output voltage. This mode of operation is called differential input, differential output mode.

The difference amplifier may also be used in a single-ended output mode. Let us ground one of the inputs, say the base of T2 via a small resistor. A positive input at the base of T_1 results in a negative output at its collector i.e. it acts as an inverting amplifier. This is referred to as the single-ended input, single-ended output, inverting mode. In this mode of operation, the current in transistor T_1 increases when its base is given a positive, potential. In order to maintain I_O constant, the current in T_2 decreases by the same magnitude. As a consequence the output voltage at the collector of T_2 will be positive. Hence, if we give the input to the base of T_1 and take the output at the collector of T_2, it works as a non-inverting amplifier.

10.3 CHARACTERISTICS OF THE DIFFERENCE AMPLIFIER

(a) Gain: Fig 10.2 represents a difference amplifier with two input signals V_1 and V_2 and one output V_O. Each of these voltages is measured with respect to the ground. Under ideal conditions; the output voltage V_O is given by

$$V_O = A_d (V_1 - V_2) \qquad \ldots. (10.1)$$

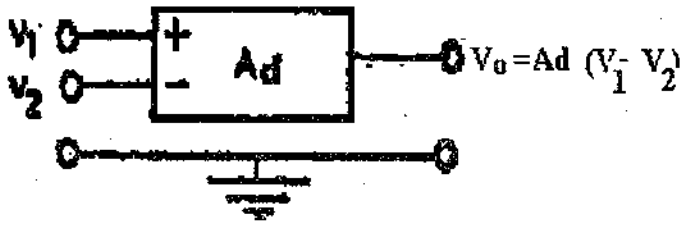

Fig 10.2: Difference Amplifier schematic Representation

Where A_d is the gain of the amplifier for the difference signal. It is called the differential gain. If $V_1 = V_2$ the output is zero under ideal conditions. Thus, any signal common to both the terminals (noise) is rejected by the amplifier.

However, in a practical difference amplifier, the output is not zero even if $V_1 = V_2$This means equation (10.1) does not hold good under practical conditions. The output voltage of a practical difference amplifier depends not only on the difference voltage $V_d = (V_1 - V_2)$ but also on V_e the voltage common to both the inputs. The voltage common to both the inputs is called the common-mode voltage. It is given by $V_C = (V_1 + V_2)/2$. The output-input voltage relation of a practical difference amplifier can be expressed as

$$V_O = A_d (V_1 - V_2) + A_C V_C \qquad \ldots(10.2A)$$

$$V_O = A_d (V_1 - V_2) + A_C \frac{V_1 + V_2}{2} \qquad \ldots(10.2B)$$

where Ac is the gain of the amplifier for the common-mode signal. For an ideal difference amplifier $A_C = 0$.

The ratio of the differential and common mode gains (A_d/A_C) indicates the effectiveness with which the amplifier rejects the voltage common to both the input signals. It is termed as the Common-Mode Rejection Ratio (CMRR) ρ

$$\text{CMRR} = \frac{A_d}{A_C} = \rho \qquad \ldots(10.3)$$

For a good differential amplifier CMRR (dB) = $20 \log_{10} | (A_d / A_C) \approx 80$ to 120 dB Combining equations (10.2) and (10.3), the output voltage of a practical difference amplifier may be expressed as

$$V_O = A_d V_d \left[1 + \frac{1}{CMRR} \frac{V_C}{V_d}\right] \qquad \ldots(10.4)$$

A rigorous analysis of the circuit (which is behind scope of this book) yields that

$$\left|\frac{A_d}{A_E}\right| = \frac{h_{fe} . R_E}{h_{ie}} \qquad \ldots(10.5)$$

An examination of the above equation shows that the difference amplifier should be designed to have a high value for CMRR. High values of CMRR are achieved by choosing transistors, having large values for h_{fe} and low values for h_{ie} along with a high resistance for R_E.

Worked example:

A difference amplifier has the following parameters:

Gain = 10,000 = A_d differential gain

V_1 = 6mV;

V_2 = 4mV

CMRR = 10,000

Calculate the output voltage. What is the error introduced in the output voltage due to the finite value of CMRR?

Ideal conditions:

A_C = O. CMRR = α

V_O = 10,000 (6mV - 4mV)

= 10,000 x 2x 10^{-03} = 20 volts.

Practical amplifier

$$V_O = A_d (V_1 - V_2) + \frac{A_d}{CMRR} \cdot \frac{V_1 + V_2}{2}$$

$$= 10{,}000 \text{ X } 2 \text{ X } 10^{-03} + \left(\frac{6+4}{2}\right) \text{X } 10^{-03}$$

$$= 20 \text{ V} + 5 \text{ X } 10^{-03} \text{ V}$$

$$= 20.005 \text{V}$$

The error voltage = 5 mV

10.4 SUMMARY

Difference amplifier has two inputs and one output terminals. Most important Characteristics of the difference amplify are the differential gain and CMRR.

10.5 MODEL EXAMINATION QUESTIONS

I. Answer the following question in detail

1. Draw the circuit diagram of a difference amplifier and explain its action.
2. Give an expression for the gain of a differential amplifier.
3. What is meant by common mode signal?
4. Define common mode rejection ratio (CMRR) for a difference amplifier.
5. What should be the magnitude of CMRR for a good differential amplifier?

10.6 REFERENCES

1. Electronic circuits	Schilling Donald
2. Integrated circuits	K R Bothkar
3. Basic Electronics	Grob and Bernard
4. Electronic principles	Malvino Albert
5. Electronic circuits	Bapat Y N
6. Linear Integrated circuits	Ray choudhary and Jain

UNIT-11: OPERATIONAL AMPLIFIER AND IT'S CHARACTERISTIC PARAMETERS

Contents:

11.0 AIMS AND OBJCTIVES

In this unit you are given an idea of operational amplifier and its parameters.

After going through this unit you can discuss the characteristics of operational amplifier under ideal conditions also.

11.1 INTRODUCTION

DC amplifiers with high gain, high input impedance, large band-width and low output impedance were originally designed to perform mathematical operations like addition, multiplication, integration, and differentiation etc,; hence the name operational amplifier. They were widely used in analogue computers and other equipment. Hence it has acquired the name 'Versatile "operational amplifier" or simply "operational amplifier".

The output voltage of an op amp is given by

$$V_O = A_O (V^+ - V^-) \qquad ...(11.1)$$

Where A_O is the open-loop gain (gain without any feedback arrangement) V_O is the output voltage V^+ and V^- are the input voltages. A_O is of the order of $10^5 \approx 10^8$ for purpose Op. Amps.

11.2 CHARACTERISTICS OF IDEAL OPERATIONAL AMPLIFIER

The following are the characteristics of an ideal op amp:

(a) Open-loop Gain $A_O = \infty$

(b) Input Impedance, $Z_i = \infty$

(c) Output Impedance, $Z_O = 0$

(e) CMRR = ∞

(f) Offset Voltage and Offset Current = 0

(g) Slew Rate = ∞

(d) Band width B = ∞ (h) Stability S = ∞

Slew rate is defined as the maximum time rate of change of the output voltage without distortion.

It can be mathematically expressed as $S = \left(\frac{dV_o}{dt}\right)_{max}$. Larger the magnitude of 'S' better will be the performance of the operational amplifier at high frequencies.

The equivalent circuit of the ideal op amp is shown in Fig. 11.1. The above characteristics make the op amp very useful. No current flows into the op amp is its input impedance is infinite.

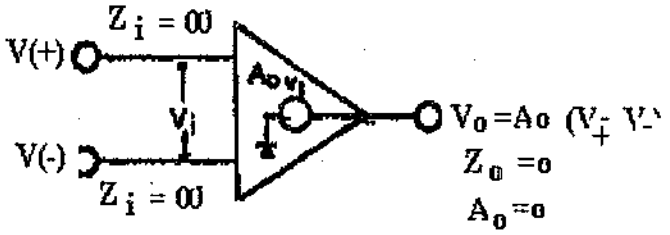

Fig 11.1 Electrical Equivalent circuit and block diagram of the ideal op. amp

The amplifiers performance is un effected by loading as its output impedance is zero. Its infinite bandwidth makes the phase difference between input and output voltages independent of frequency. The performance of the amplifier depends only on the external feedback network as its gain is infinite.

The characteristics cited above are only ideal. It is not possible to achieve them in practice. However op amps presently being fabricated using integrated circuit-technology (the whole circuit is engraved on a silicon chip). Possess characteristics very closer to the ideal ones. The characteristics of a real op. amp are presented below:

(a) Open-loop gain	A_O:	10^5-10^8
(b) Gain-Bandwidth product	:	100 MHz
(c) Input impedance	Z_i:	10^5 to 10^{12} for general purpose Op. Amps
		$\approx 10^{16}$ ohms for special purpose MOS FET input Op. Amps
(d) Output impedance	Z_O:	1-10 ohms. W - 100 Ω
(e) CMRR	:	80-140 dB
(f) Off set voltage	:	few μ V
and off set current	:	few η A
(g) Slew rate	: ≈	IV/ μ sec

11.3 OPERATIONAL AMPLIFIER: BLOCK DIAGRAM

It is not essential to know what is inside the IC op amp in order to use it profitably. However, the user feels comfortable when he has some idea of its design. He will be' in a position to appreciate its limitations.

The block diagram of a general purpose IC op amp is shown in Fig 11.2. The first stage in all types of op amps is the differential amplifier. It has two input terminals. This amplifies the difference in the voltages applied between its input terminals. The differential amplifier converts the input voltages into output currents or output voltages. The second amplifier converts these currents or voltages into a single-ended current or voltages. -Hence it is called differential-to-single-ended converter. This single ended output current is converted into voltage by the third amplifier. In the final output stage an output driver a low power amplifier is used to boost the power and to provide low output impedance.

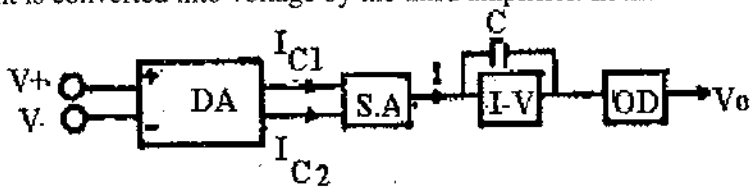

Fig 11.2 Block diagram of the basic op amp
DA: Difference Amplifier; S.A: Second Amplifier
I-V: Current - to - voltage Converter;

11.4 FEEDBACK ARRANGEMENTS

The schematic, diagram of the op amp is shown in Fig 11.3. It has two input terminals. The terminal marked (-) is called the inverting input terminal.

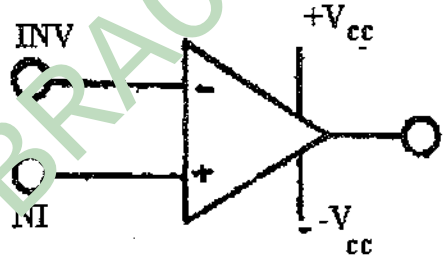

Fig 11.3 op amp-Schemeatic Diagram
INV: Inverting
NI: Non-Inverting

The other terminal marked (+) is call the non-inverting terminal. The + and - signs indicate the phase relation between the input and output voltages. A positive voltage applied to the inverting terminal results in a negative output voltage. There is a phase inversion between the input and the output signals. The same voltage applied to the non-inverting terminal results in positive output. The output signal is in phase with the input signal.

The battery or power supply is used to energise the op amp and the ground terminals are not usually shown in the schematic diagram.

The operational feedback arrangements are shown in Fig 11.4a shows the inverting amplifier configuration while Fig. 11.4b shows the non-inverting amplifier configuration. In both the configurations, Z_f connects the input and output terminals i.e. the output is fed back via Z_f Hence it is called the feedback impedance. In this type of feedback, the earth terminal is common to the input and the output circuits. In the conventional feedback that was discussed in UNIT-2.There is no such common terminal.

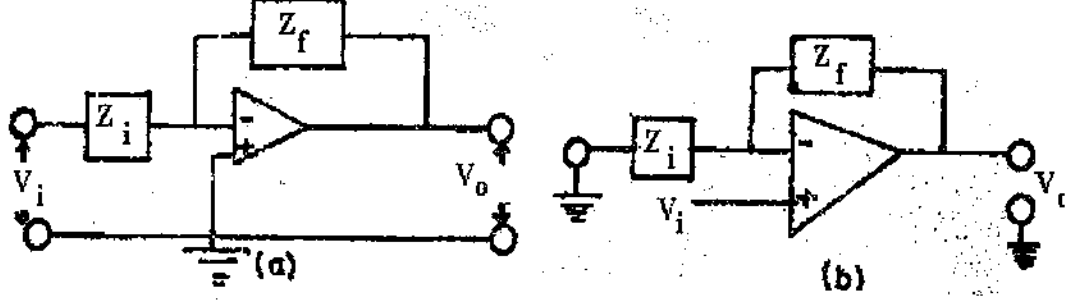

Fig 11.4 op Amp (a) Inverting Configuration

(b) Non-inverting configuration

The closed – loop gain of the op. amp in Inverting Configuration is given by

$$\frac{V_O}{V_I} = A_V = -\frac{Z_f}{Z_i} \qquad \ldots(11.2).$$

The closed loop gain of the op. amp in Non-Inverting configuration is given by

$$\frac{V_O}{V_I} = A^+_O = \left(1 + \frac{Z_f}{Z_i}\right) \qquad \ldots(11.3)$$

11.5 OPERATIONAL AMPLIFIER PARAMETERS

Every op amp has a set of special specifications. The selection of an op amp for a particular application is made on the basis of an examination of these specifications. This section introduces the reader to various specifications and their important parameters normally used in Op. amps.

(a) Open-loop gain (A_O): It is the gain of the op amp without any feedback. It is defined as the ratio of the change in the output voltage to the change in the differential input voltage. This is normally specified at DC. The op amp is very rarely used under open-loop conditions. However, the open-loop gain is significant as it determines the accuracy of the amplifier with feedback (closed-loop).

(b) Common-mode voltage gain (Ac): It is the ratio of the change in the output voltage to the change in the input voltage when both the input terminals are tied together. Ac is usually thousands of times smaller than A_O.

(c) Common-mode rejection ratio (CMRR): when two identical signals (equal voltages of the same phase) are applied to both the inputs simultaneously or a single common voltage is applied to the two inputs tied together are called common-mode signals. For an ideal op amp, the output voltage should be zero if there" is no difference in the amplitudes phases of the two signals applied to its inputs. In practical op amps, because of slightly different gains for the inverting and non-inverting inputs, there will be some finite but small output even when the input voltages are exactly indentical.

It is desirable to keep A_C to be very low value. It is only then that the amplifier will be able to reject noise common to both the terminals. The ability of an op amp to reject the common mode signals is indicated by the common-mode rejection ratio (CMRR). It is defined as the ratio of the differential and common-mode gains.

Example

$$CMRR = |A_d / A_C| \qquad \ldots(11.4A)$$

CMRR is also expressed in decibles (dB), If $|A_d / A_C| = 10{,}000$, then $\ldots(11.4B)$

$$CMRR = 20 \log_{10} 10{,}000 = 100 \text{ dB} \quad \ldots(11.4C)$$

(d) Bandwidth (B): The open-loop bandwidth. is defined as the frequency at which A_O falls by 3dB from its maximum value at DC (Fig. 11.5). It represents the range of frequencies over which the gain of the op

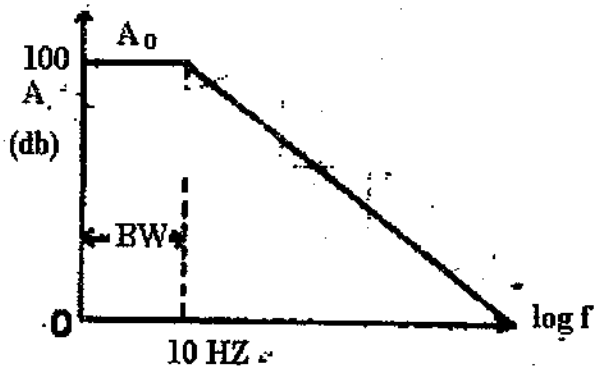

Fig. 11.5 Frequency response of the op amp BW: Band width

amp is reasonably constant, the gain, as indicated in the figure, is expressed in decibels (dB). (For example, if the gain is 100, its value in (dB) is 20 log 100 = 40 dB; if the gain is 1000; its dB value is 20 log 1000 = 60 dB). The curve shown in Fig. 11.5 is called the Bode plot.

Example:

The. dc gain of an op amp is 100 dB. Its value at 10 Hz is 97 dB. Hence the Band width is 10Hz. ...(11.5)

(e) Slew rate (S): The capacitors in the op amp limit the rate at which the output voltage can change. The slew rate is defined as the maximum time rate of change of the output voltage without distortion. It is specified in volts/microsecond. Typical value for slew rate is 1 V / μ sec. ...(11.6)

The lower values of slew rate results in distortion of large amplitude signals even though they are within the passband of the amplifier. For sine waves.

$$V_O = V_P \sin 2\Pi ft \quad \ldots(11.7)$$

$$\frac{dV_O}{dt} = 2\ \Pi f V_P \cos 2\ \Pi\ ft \quad \ldots(11.8)$$

Thus for a given peak value V_P of the output voltage, there is a maximum frequency 'f 'for the signal to appear at the output without distortion.

(f) Off-set voltage $(V_{OS})_O$: The op amp, in general, gives an output voltage called the offset voltage even if the input terminals are earthed. This is due to lack of symmetry mismatch in the input differential stage of the op amp during fabrication process. The output voltage may be considered as arising out of a small input voltage $(V_{OS})_i$ called the input offset voltage in series with one of the input leads. The input offset voltage may be defined as the differential dc input voltage required to zero null the output with no input signal.

In IC op amp, the offset voltage ranges from 1 to 10mV. It gets amplified and saturates the output. Hence it is necessary to balance the offset voltage in certain applications.

(g) Bias currents: Two bias currents I_b^+ and I_b^- flow into the input terminals (Fig. 11.6) even when the input voltages are zero. These are the currents used to bias the input transistors. In well balanced amplifiers with equal input impedances, the effects of these

currents largely cancel. Hence it is the difference between the bias currents i.e., I_b^+ and I_b^- called the offset current that is of interest. Typical values are in the range I=100 nanoamperes

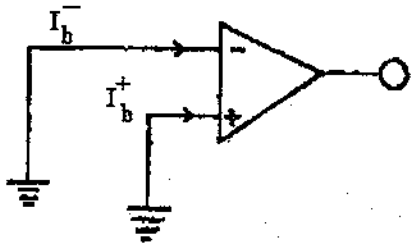

Fig: 11.6 Bias currents

11.6 SUMMARY

DC amplifiers with high gain, large bandwidth, high input impedance and low output impedance are called operational amplifiers. They can be used for carrying out certain mathematical operations and hence the name operational amplifiers is given to them. The main characteristics of any op amp are the loop gain, bandwidth, common mode rejection ratio, slew rate, offset voltage and off set currents.

11.7 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Give the block diagram of an operational amplifier and explain the function of each block.

II. Answer the following questions briefly.

1. What are the characteristics of an ideal operational amplifier? How far are they achieved in practice?
2. Define (1) Offset Voltage (2) offset currents and (3) CMRR of an op amp.

III. Solve the following problems.

1. The differential gain of an op amp is 20,000. Its CMRR is 100 dB, what is the common mode gain [Ans: 5]
2. The maximum undistorted output voltage of an op amp at 1 MHz is 10 V (peak). Compute the slew rate of the amplifier. .

11.8 REFERENCES

1. Electronic circuits — Schilling Donald
2. Integrated circuits — K R Bothkar
3. Basic Electronics — Grob and Bernard
4. Electronic principles — Malvino Albert
5. Electronic circuits — Bapat Y N
6. Linear Integrated circuits — Ray choudhary and Jain

UNIT-12: OPERATIONAL AMPLIFIER CONFIGURATIONS-ANALYSIS

Contents:

12.0 AIMS AND OBJECTIVES

This unit introduces you to

1) the simple model for the ideal Op Amp
2) the method of using Op Amp to carryout mathematical operations such as summing, scale changing(multiplying and dividing)device integrator and differentiator.

After going through this unit you will be able to

1) analyse different configurations of Op Amp and

2) derive an expressions *for* closed loop gain for different configurations.

12.1 INTRODUCTION

Under ideal conditions the voltages at the inverting and non-inverting terminals of an op Amp are virtually equal. This is called the 'principle of virtual equality. This principle enables us to analyse different op Amp configurations in a simple way. This principle leads us to the concept of virtual ground. The gain of the op Amp with the feed back network is called the closed loop gain.

12.2 SIMPLE MODEL FOR THE IDEAL Op-Amp

The output voltage V_O of an ideal op amp is given by

$$Vo = A_O (V^+ - V^-_E) \qquad ...(12.1)$$

where V^+ and V^- are me voltages applied to the non-inverting and inverting input terminals respectively. With finite values for V_O and very large value for A_O we have

$$\frac{V_o}{A} = V^+ - V^- \approx 0$$

or

$$V^+ \approx V^- \qquad ...(12.2)$$

This condition leads us to the conclusion that the voltages at the two input terminals are virtually equal. This is called the "Principle of Virtual Equality". It is a powerful approach to analyse different op amp configurations. .

If the non-inverting terminal is grounded, according to the above principle, the inverting input terminal is virtually at the ground potential (Fig. 12.1).

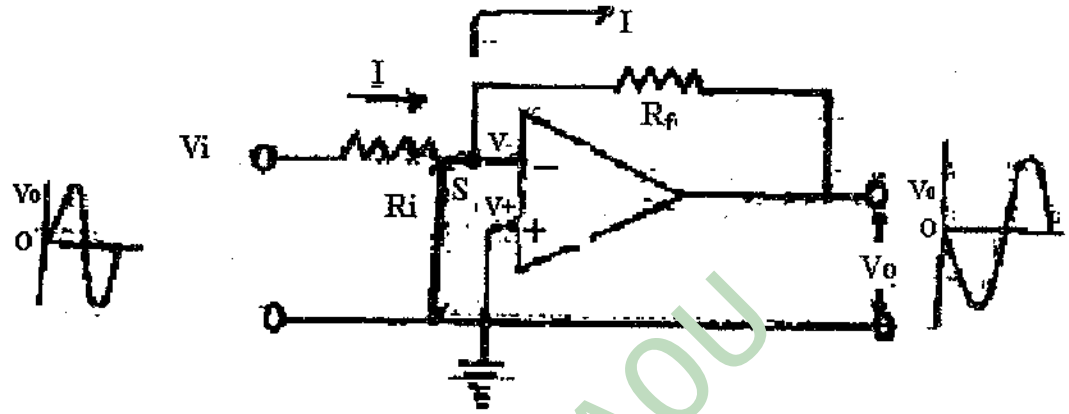

Fig 12.1 Inverting Amplifier,
S- Virtual ground

The point S is called the virtual ground. This concept is very useful in many op amp circuits. For example, even if two (or. more) resistors are connected together at this common virtual ground, they will not cause any significant voltage coupling between the input signal sources. This is because there is essentially (or virtually) no voltage present at this common terminal point. The virtual ground isolates the input signal sources from each other.

12.3 INVERTING AMPLIFIER – SCALE CHANGING

The basic op amp inverter is shown in Fig. 12.1 since $V^+ = 0$, we have $V^- = O$. The current through R_1 is given by $I = V_i/R_i$ Since we assume infinite input impedance, no current flows into the op amp. As a result the same current (I) flows through R_i and R_f the output voltage is given by

$$I = \frac{V_i}{R_i}$$

$$V_O = -IR_f = -V_i \frac{R_f}{R_i} \qquad ...(12.3)$$

The ideal closed-loop gain G is given by

$$G = \frac{V_O}{V_1} = -R_f/R_i \qquad ...(12.4)$$

There is a phase inversion between the input and output signals in this configuration. Thus the op amp's closed-loop gain is dependent only on the ratio of the feedback and input resistors. Hence it is used for multiplication. For example if $R_f/Ri = 10$, the input voltage is multiplied by a factor of 10. On the other hand if $R_f/Ri = 1/10$, the input is divided by factor 10. Thus it can be used both as a multiplier and a divider. Hence, in general it is called a scale-changing amplifier.

Let us now study the virtual ground in detail by considering a specific example shown in Fi2. 12.2 it is

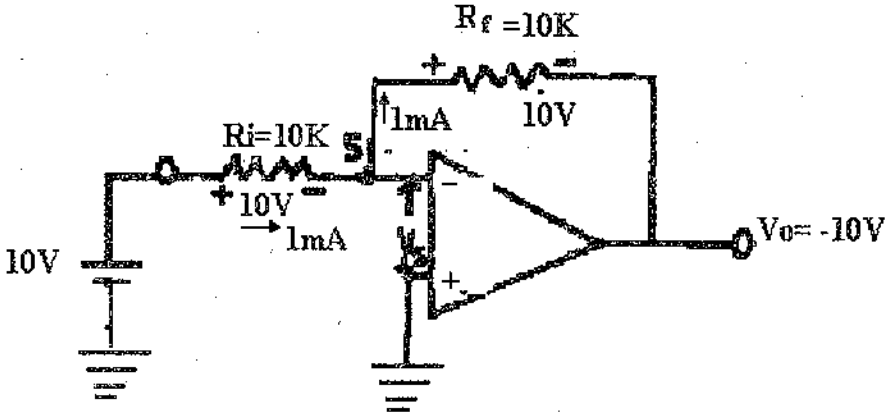

Fig 12.2 Virtual ground 100 μ V at S is virtually grounded

a unity gain inverter. The output voltage

$$V_O = \frac{-R_f}{R_i} V_i = -\frac{10}{10} \times 10 = -10 \text{ volts}$$

The open-loop gain of the op amp used is 100,000. To produce an output voltage of -10v, there should be a voltage V s between the two input terminals given by

$$V_S = \frac{-V_o}{A} = \frac{10V}{100,000} = 100\mu \text{ V}$$

Thus a small potential difference of 100 μv exists between the Real Ground and the Virtual Ground. Hence, it can be assumed that the virtual ground 'S' is also at ground potential.

12.4 SUMMING AMPLIFIER

The circuit show in Fig. 12.1 can be modified as shown in Fig. 12.3, which has three input sources. The working of this adder configuration can be understood using the concept of virtual equality. Since the non-inverting terminal is earthed that is at, $V^+ = 0$.

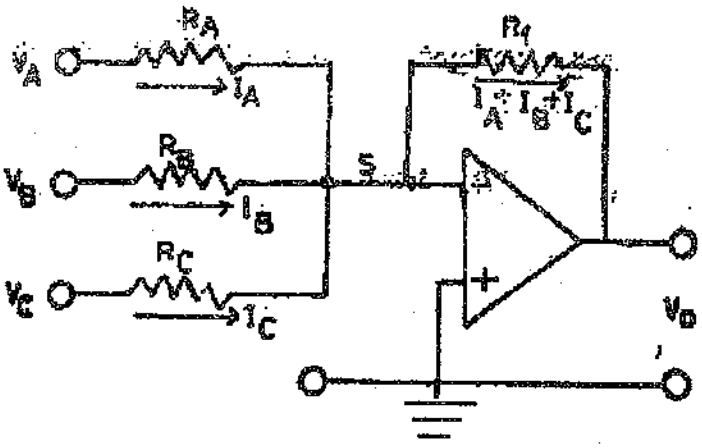

Fig 12.3 Summing amplifier

$$V_o = -R_f (I_A + I_B + I_C) = R_f I_S = -R_f (I_f + I_Q) \approx -R_f I_f \text{ since } I_a << I_f$$

$$= R_f \left(\frac{V_A}{R_A} + \frac{V_B}{R_B} + \frac{V_C}{R_C} \right) \quad \ldots (12.5)$$

If $R_A = R_B = R_C = R_f$ we have

$$V_O = (V_A + V_B + V_C) \quad \ldots (12.6)$$

The output voltage is equal to the sum of the three input voltages

If $R_A = R_B = R_C = 3R_f$

$$V_o = -\frac{1}{3} (V_A + V_B + V_C) \quad \ldots . (12.7)$$

i.e. it acts as an averaging circuit. Weighted average of the three inputs may be obtained by making

$$R_C = R_f = -\frac{1}{3} R_A \text{ and } R_B = \frac{1}{2} R_A$$

Then we have

$$V_o = -\frac{1}{3} (V_A + 2V_B + 3V_C) \quad \ldots . (12.8)$$

In computing the average, we have given V_0 twice as much weight as V_A and V_C thrice as much weight as V_A. Thus the output voltage is the weighted average of three voltages.

12.5 NON-INVERTING AMPLIFIER

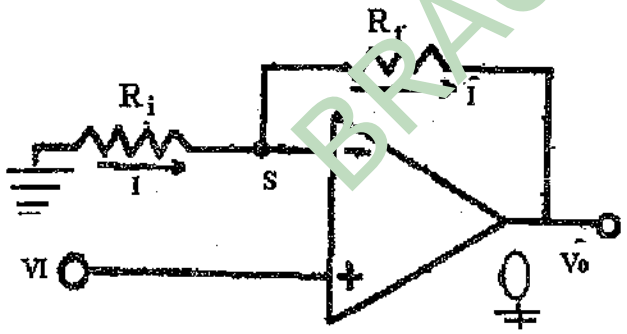

Fig 12.4 Non-inverting Amplifier

Fig. 12.4 show the Op ams in non-inverting configuration In this circuit, we have, according to the principle of virtual equality

$$V^+ = V_i = V^-$$

Then

$$I = \frac{V_i}{R_i}$$

Since I also flow through R_f we have

$$V_O = V_i + IR_f$$

$$= V_i + V_i \frac{R_f}{R_i}$$

$$= V_i \left(1 + \frac{R_f}{R_i} \right). \quad \ldots (12.9)$$

There is no sign change (the phases of the input and the output are the same). It may be noted that in this configuration no current is drawn from the source V_i (unlike the

12.6 CURRENT FOLLOWER

The circuit shown in Fig. 12.5 gives an output voltage proportional to the input current. Thus it acts as a current to voltage converter.

$$V_O = - IR_f \qquad ...(12.10)$$

Considering that $A_O = 10^5$, and a value of 100 kΩ for R_f leads to one ohm input resistance.

This configuration is an ideal current measuring device, which is useful for measuring very small currents of the order nano amperes and less

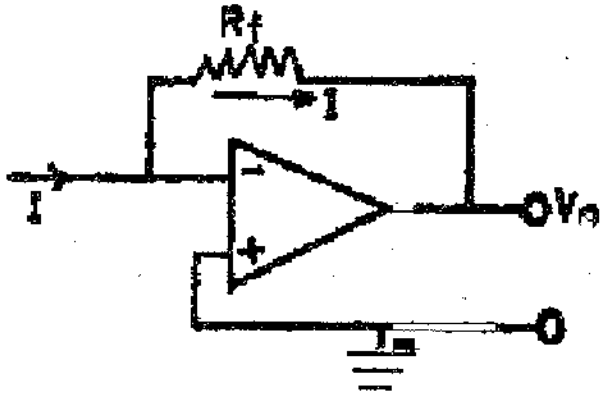

Fig. 12.5 Current Follower

12.7 VOLTAGE FOLLOWER

The voltage follower circuit shown in Fig. 12.6 can be used to match a source of very high impedance to a load of low impedance.

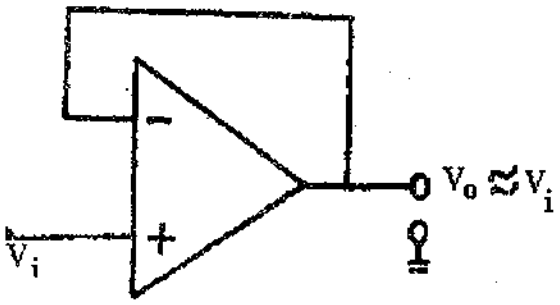

Fig. 12.6 Voltage follower

The entire output signal is fedback into the inverting input. The input signal is connected to the non-inverting input. According to the principle of virtual equality

$$V^- = V^+ = V_i \approx V_O \qquad ...(12.11)$$

This circuit is called a voltage follower, because the output voltage is almost equal to the input voltage. This configuration is similar to an emitter follower in BJT or a source follower in FET amplifiers. This is due to the fact that large A_O does not allow a large differential voltage to exist.

The circuit diagram of an Op amp (Active) integrator is shown in Fig. 12.7. Since, the non-inverting terminal is also earthed. Hence the inverting input is at the ground potential. The current I through R is given by V_i/R. The voltage across the capacitor is equal to the output voltage. It is given by

The charge accumulated on the capacitor C is given by $Q = -C V_O$ or $-V_O = \frac{Q}{C}$

and further $Q = \int I_f dt =$

$$\therefore -V_O = \frac{1}{C}\int I_f dt$$

from the circuit the current following in the input circuit is given by

$$I_i = \frac{V_i}{R}$$

Since $I_i = I_f$

$$\therefore -V_O = \frac{1}{C}\int \frac{V_i}{R} dt$$

$$-V_O = \frac{1}{CR}\int V_i dt$$

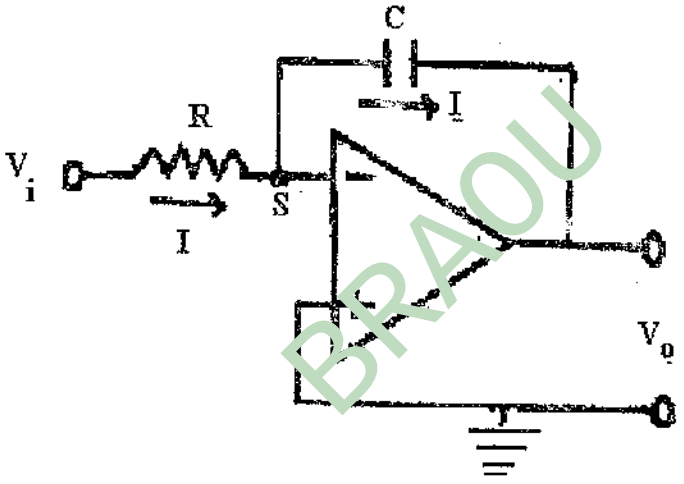

Fig. 12.7 op Amp Integrator

The time constant RC = T is called the characteristic time of the integrator $\frac{1}{T}$ gives the gain of the integrator (This is called an active integrator as the active element (op amp) is used in achieving integration. If the time constant of the integrator RC is made equal to 1 sec (R=1 mΩ i.e., $1X10^6$ ohms and c = 1 mF i.e., $1 X10^{-6}$; then RC = 1 sec) then the expression (12.11) reduces to

$$-V_O = \int V_i dt \qquad \ldots(12.12)$$

If the input of the active integrator is a dc voltage, V its output is given by

$$Vo = -\frac{V_i}{RC} \qquad \ldots(12.13)$$

The output voltage varies linearly with time i.e. it produces a ramp voltage. If the input is a square wave, the output is a triangular wave.

12.9 Op AMP DIFFERENTIATOR

Fig 12. 8 shows the op amp (active) differentiator. Since the non-inverting terminal is grounded, point S is at the virtual ground. Hence the current through the capacitor is given by

$$\frac{dQ}{dt} = I_i = c\frac{d(V_i)}{dt} \qquad ...(12.14)$$

where $Q = C V_i$

The feedback current I_f is given by

$$I_f = \frac{-V_O}{R} or V_O = -RI_f$$

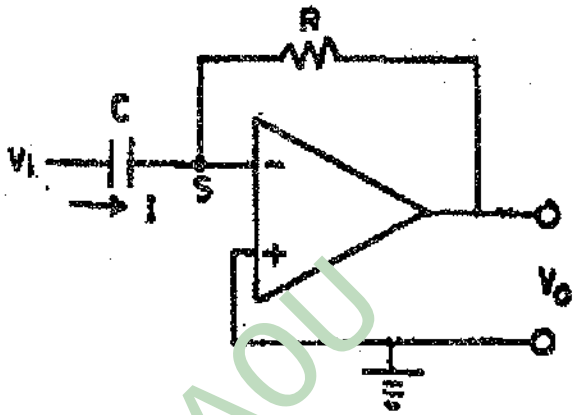

Fig. 12.8 Op Amp Differentiator

Since $I_f = I_i$, we have

$$\therefore V_O = RI_f = RI_i$$

Subtracting for I_i from equation12.14 in the above equation, we get

$$Vo = -RC\frac{dV_i}{dt} \qquad ...(12.15)$$

The output voltage is proportional to the differential of the input voltage.
If we make the time constant of the differentiator RC = 1Sec(i.e., $r = 1X10^6$ ohms and

$C = 1X10^{-6}F$ the equation 12.15 reduces to $V_O = -\frac{dV_i}{dt}$ ...(12.16)

12.10 SUMMARY

The principle of virtual equality leads us to the concept of virtual ground. The Op Amp can be used as a scale changer i.e., multiplier or divider, summing device, integrator and differentiator.

12.11 MODEL EXAMINATION QUESTIONS

I. Answer the following questions briefly.

1. Arrive at the principle of Virtual equality. What is Virtual ground?
2. Describe how an op Amp can be used to add three voltages. Give the necessary circuit diagram.
3. Explain the working of voltage and current followers.
4. Discuss the action of active integrator and differentiator.

12.12 REFERENCES

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2. Op-Amps and linear Integrated circuits — Ramakanth Gayakwad.
3. Operational Amplifiers and linear Integrated circuits — Coughlin Robert and Driscoll Fredder

12.13 GLOSSARY

Op Amp	:	DC amplifier with high gain, large bandwidth high input impedance and low output impedance.
Open-loop gain	:	Gain without the feedback loop
Bandwidth	:	The band of frequencies over which the gain of The Amplifier falls within a specified fraction of its maximum value.
Input impedance	:	Impedance of a circuit or device presented at its input.
Output impedance	:	Impedance presented at the output of an electronic Circuit or a device
Constant current source	:	A circuit whose output current is independent of voltage.
Integrated circuit	:	A complete circuit that is manufactured as a Single Package. The whole circuit including transistors, resistors, and capacitors is engraved on a single silicon chip.

BLOCK – IV

OSCILLATORS AND MULTIVIBRATORS

UNIT -13: OSCILLATORS: BARKHAUSEN'S CRITERION

Contents:

13.0 AIMS AND OBJECTIVES

This unit explains the

1) Method of converting an amplifier into oscillator by using feedback circuit and

2) Method of sustaining oscillations in oscillators

After going through this unit you will be in a position to discuss

1) The feedback mechanism that results in oscillations

2) Barkhausen Criterion for a general oscillator arrangement and

3) Principle of sustaining the oscillations

13.1 INTRODUCTION

A fraction of (β) of the output voltage (V_O) of the amplifier can be fed back into its input circuit through a feedback network, which may consist of resistance - capacitance combination or capacitance inductance combination. The feedback network introduces phase difference between the input and feedback voltage of the amplifier. The phase difference depends upon the frequency. If this feedback is positive, oscillations are generated in the amplifier. Barkhausen condition is to be satisfied for sustaining the oscillations.

13.2 POSITIVE FEEDBACK AND OSCILLATOR – MECHANISM

An amplifier amplifies the given signal. A fraction of the output signal may be fed back into the input of the amplifier to alter its behavior. If the input and the feedback voltages are in phase with each other the feedback is called positive feedback. Positive feedback may be utilised to produce oscillations.

Fig.13.1 shows an amplifier with feedback arrangement the amplifier with an open loop gain A is assumed to be stable. It-introduces a phase shift of 0^0 to 180^0 between its input and output voltages. The output of the amplifier (V_o=Av_i) is connected to feedback network. The feedback network consists of resistance-capacitance or capacitance-inductance combination. It reduces the voltage given to it by a fraction β know as the feedback ratio. If V_O is its input voltage, its output is βV_O In addition. it shifts the phase of the signal passing through it. The phase shift produced depends on the frequency. At a particular frequency, the total phase shift becomes zero or 360°.Thus feedback network determines the frequency of oscillations

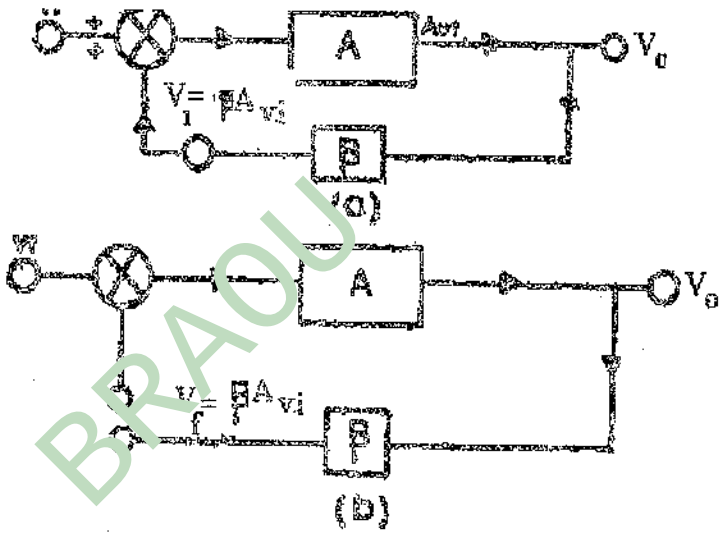

Fig. 13.1 Feedback arrangement for oscillations

Let us now try an imaginary experiment. Let the feedback loop be opened as shown in Fig. 13.1 b. The signal (V_i) will be amplified *to* give ($A .V_i$) at the output of the amplifier. It is then passed into the feed back network. The output of the feedback network is β V_o = β Av_i. This is called the feedback voltage V_f .The phase of V_f is shifted (with repsect to V_i) because of the reactive elements in the feedback network. If the gain A of the amplifier is large enough (which is usually the case) *it* is possible *to* make the magnitude of V_f equal to that of V_i Let us, assume that we have, achieved this.

If the frequency of Vi is varied, the phase of V_f changes. At some frequency f_o (or frequencies) the-phase of V_f will be identical to that of Vi. At this frequency the total phase shifts over the loop (Consisting *of* the amplifier and the feedback loop) is zero. At f_O the feedback voltage V_f is identical *to* the input voltage Vi in both magnitude and phase.

$V_f \equiv V_i$ both in magnitude and phase ...(13.1)

or $V_f = V_i + j\,\hat{O}$ ...(13.2)

If we now remove the external source and connect V_f to the input of the amplifier. it continues to provide the same output signal V_O as before since the amplifier has no means

of distinguishing the source of input signal, i.e. it produces oscillations at frequency f_0

13.3 BARKHAUSEN'S CRITERION

The result of the imaginary experiment described above may be summarised as stated below.

The frequency at which an oscillator will operate is the frequency for which the total phase shift introduced, as the signal proceeds from the input terminals, through the amplifier and through the feedback back network, and back again to the input, is exactly zero or an integral multiple, of 2π.

To maintain (or substrain) the oscillations at any desired frequency f_0, the magnitude of the loop gain over the network should be equal to unity and the total phase shift "ϕ" should be zero. The loop gain is the product of the open loop gain of the amplifier "A" and the feedback ratio "β". Both the conditions stated above may be expressed (using phasor and complex number notations respectively)

$$A\beta = 1+j\,\hat{O} \qquad \text{.... (13.3)}$$

It is called the Barkbausen's criterion for maintenance of oscillations.

13.4 RC OSCILLATORS

To produce audio frequency oscillations using L-C is very difficult as their values become impractically large. Hence R-C combinations are used in the feedback network of an operational amplifier. Wien-bridge and Phase shift, oscillators are discussed in this unit.

To produce radio frequency oscillations, using R-C is very difficult as their values become impractically small and hence L-C combination is used as in the tank circuit of the amplifier. Gain of the amplifier is maximum at the resonant frequency of this tuned circuit. A part of the voltage across the tuned load is fed back to obtain oscillations. In this case the open loop A is a sensitive function of frequency. Colpitt's and Hartley oscillators are discussed in this unit.

13.5 WIEN BRIDGE OSCILLATOR

The circuit diagram of the popular Wien-bridge oscillator is shown in Fig. 13.2. The op amp with Z_1 and Z_2 constitutes the feedback network connected in the non-inverting configuration. Its gain

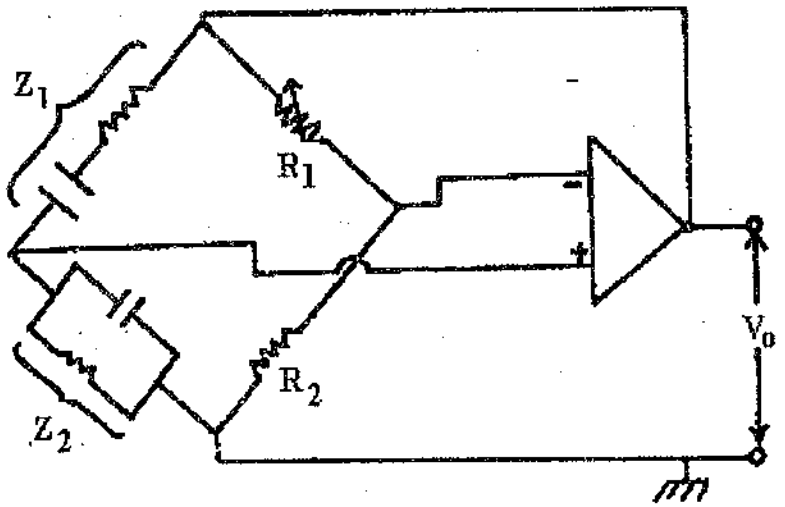

Fig 13.2 Wien-bridge oscillator R_1, R_2, Z_1 and Z_2 Constitute the bridge

$A_V = \left(1 + \frac{Z_2}{Z_1}\right)$. This feedback network does not introduce any phase difference between its input and output. Hence, it applies the positive feedback

The output of the amplifier V0 is applied to the voltage divider network consisting of Z_1 and Z_2. The positive feedback fraction is given by

$$\beta^+ = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2} = \frac{1}{1 + \frac{Z_1}{Z_2}} \qquad \text{.... (13.4)}$$

The values of Z_1 and Z_2 are

$$Z_1 = [R \parallel X_C] = R + \frac{1}{j\varpi C} = \frac{1 + j\varpi CR}{j\varpi C} \qquad \text{... (13.5)}$$

Where $X_C = \frac{1}{J\varpi C}$

and $$Z_2 = [R \parallel X_C] = \frac{R}{1 + j\varpi CR} \quad \left(\because \frac{1}{Z_2} = \frac{1}{R} + j\varpi C\right) \qquad \text{...(13.6)}$$

Substituting for Z_1 and Z_2 in eqn (14.2), we get

$$\beta^+ = \frac{1}{\frac{Z_1}{1 + Z_2}} = \frac{1}{3 + j\left(\varpi CR - \frac{1}{\varpi CR}\right)} \qquad \text{...(13.7)}$$

Since A_V is a real number, β^+ should also be a real number (with zero phase shift) to satisfy the Barkhausen's criterion (eqn. 13.3). This requires that the coefficient of the imaginary term in eqn. (13.7) should be equal to zero i.e.

$$\left(\varpi CR - \frac{1}{\varpi CR}\right) = 0 \qquad \text{...(13.8A)}$$

or $\varpi_o CR = \frac{1}{\varpi_o CR}$ *or* $\varpi_o^2 = \frac{1}{(CR)^2}$ or $W_O = \frac{1}{CR}$

i.e., $$f_O = \frac{1}{2\pi CR} \qquad \ldots(13.8B)$$

The above equation indicates that β^+ is a real number only at the above frequency. Hence, from equation 13.7 the value of β at this frequency is given by

$$|\beta^+| = \frac{1}{3} \qquad \ldots(13.9)$$

To satisfy the condition

$$|\beta^+ A_v| = 1 \qquad \left|\frac{1}{3} A_v\right| = 1 \text{ or } A_V = 3$$

the gain of the amplifier A_V should be at least 3 i.e.

In order to maintain the gain of the amplifier to be stable at 3, the open loop gain A_V is designed to be much larger than 3 and a balanced bridge arrangement with certain amount of negative feedback is applied through R_1 and R_2 network connected in the inverting configuration. Hence, the negative feedback ratio should be

$$\beta^- = \frac{1}{3} = \frac{R_2}{R_1 + R_2}$$

or $$R_1 = 2R_2 \qquad \ldots(13.10)$$

This is the condition for maintenance of oscillations.

In practical situations R_2 may be a thermistor whose resistance decreases with increasing temperature. If for any reason the output voltage increases, the negative feedback also increases, thus decreasing the gain A_V. It thus reduces the output voltage and maintains a constant level. The similar argument holds good for decrease in the output voltage.

13.6 PHASE SHIFT OSCILLATOR

The circuit diagram of the phase-shift oscillator is shown in Fig. 13.3. The inverting configuration is used here i.e. the amplifier produces an output which is 180^0 out of phase with the input. In order to satisfy the Baskhausen's criterion, the total phase shift should be zero. Hence, the feedback network should be designed to introduce an additional phase lag or lead by 180^0. The additional phase shift of 180^0 is obtained using the CR network. The output of the amplifier acts as input to the feedback network. Its output is fed back to the amplifier.

It can be shown that the feedback network introduces a phase difference of 180^0 only at a frequency f_O. Applying Kirchoff's voltage laws to the network and on simplification, the feedback ratio is given by (a detailed treatment of this network analysis is beyond the scope of this book).

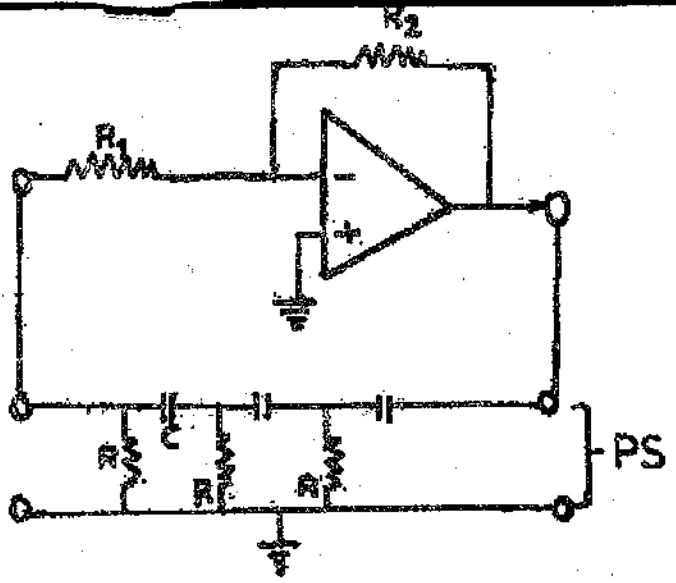

Fig. 13.3 Phase Shift Oscillator
PS-Phase Shifting network

$$\beta^{+} = \frac{1}{(1-5X^2)+j(X^3-6X)} \qquad ...(13.11)$$

where $X=\frac{1}{\varpi\, CR}$ substituting for

$$\beta^{+} = \frac{1}{1-5\left(\frac{1}{\varpi CR}\right)^2 + j\left[\left(\frac{1}{\varpi CR}\right)^3 - 6\left(\frac{1}{\varpi CR}\right)\right]} \qquad ...(13.12)$$

At resonance, the total phase shift introduced between the input and the output signal is zero. Hence, the coefficient of the imaginary part should be zero.

$$\therefore \left[\left(\frac{1}{\varpi CR}\right)^3 - 6\left(\frac{1}{\varpi CR}\right)\right] = 0 \qquad ...(13.13)$$

$$\text{or } \left(\frac{1}{\varpi CR}\right)^2 = 6 \qquad ...(13.14)$$

$$\varpi^2 = \frac{1}{6(CR)^2}$$

$$\varpi = \frac{1}{\sqrt{6}CR} \text{ or } \frac{1}{\varpi CR} = \sqrt{6} \qquad ...(13.15)$$

$$\text{or } f = \frac{1}{2\pi\sqrt{6}(CR)} \qquad ...(13.16)$$

Considering the real part

$$\left|\beta^{+}\right| = \frac{1}{\left[1-5\left(\frac{1}{\varpi CR}\right)^2\right]} \qquad ...(13.17)$$

substituting for $\left(\frac{1}{\varpi CR}\right) = \sqrt{6}$ from equ. (13.15) in equ. (13.17).

$$|\beta^+| = \frac{1}{\left[1-5\left(\sqrt{6}\right)^2\right]}$$

$$= \frac{1}{[1-5(6)]}$$

$$= \frac{1}{(1-30)} = -\frac{1}{29}$$

$$|\beta^+| = \frac{1}{29} \qquad \ldots(13.18)$$

since the loop gain $|A\phi| = 1$

$$|A| = \frac{1}{\beta^+} = \frac{1}{1/29} \quad = 29 \qquad \ldots(13.19)$$

The gain of the amplifier should be at least 29 in order to maintain the oscillations. Normally, the open loop gain of amplifier is designed to be much larger than 29 and certain amount of native fed is also introduced to reduce the gain to 29.

13.7 SUMMARY

Using a feedback circuit an amplifier can be converted into an oscillator. Barkbausen criterion is important for a general oscillator arrangement. The loop gain is the product of the open loop gain of the amplifier A and the feedback ratio β.

To produce audio frequencies using LC is very difficult as the L values become practically large. Hence RC combinations are used in the frequency determining feedback network of an operational amplifier. Two possible oscillators are Wienbridge and Phase shift oscillators.

13.8 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the circuit diagram of the Weinbridge oscillator and explain its action. Give the necessary theory.
2. What should be the minimum open loop gain of the amplifier for a Weinbridge oscillator?
3. Draw the circuit diagram of phase shift oscillator.
4. What should be the minimum open loop gain of the amplifier for a phase shift oscillator?

II. Answer the following questions briefly.

1. Arrive at the general Barkbausen criterion for oscillations.
2. Arrive at the condition for maintenance of oscillation in RC oscillators.

13.9 REFERENCES

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UNIT - 14: LC OSCILLATORS

Contents:

14.0 AIMS AND OBJECTIVES

This unit introduces you the concept of LC Oscillators and the working of Hartley's and Colpitt's oscillators.

After going through this unit you will be able to derive

1) The expression for the frequency of Oscillations and
2) The condition for the maintenance of Oscillation

14.1 INTRODUCTION

Many oscillators at radio frequencies employ a tapped high Q, parallel LC circuit as the frequency-determining element. It is shown in Fig. 14.1. These circuits have some interesting properties

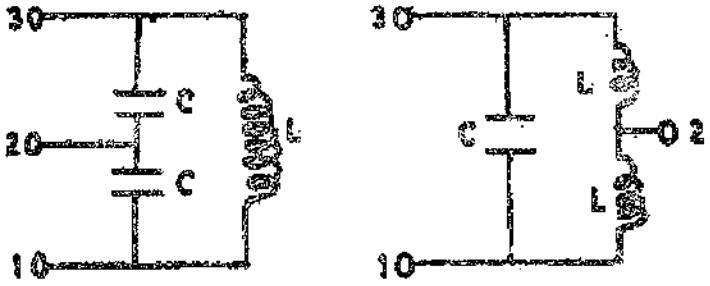


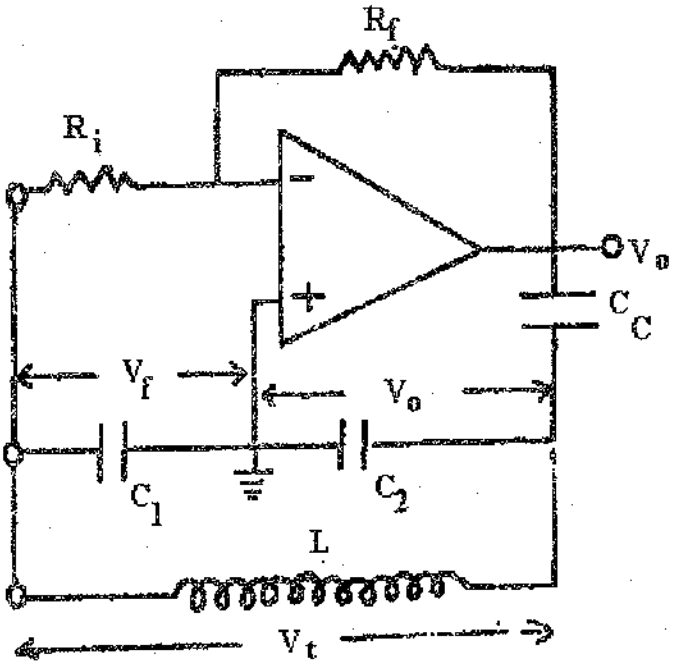
Fig. 14.1 Resonant Circuits

At the resonant frequency, they exhibit zero phase difference between the applied voltage and the resulting current. Hence, they may be employed as feedback networks in oscillators. In such high-Q circuits, the voltages at each end of the circuit (point 1 and 3) relative to the 1 (point 2) are 180^0 out of phase at the resonant frequency. These properties are used realisation of LC oscillators.

14.2 THE COLPITTS OSCILLATOR

The circuit diagram of the Colpitt's oscillator is shown in Fig. 14.2. Here, we use

inverting configuration of the op amp. Its gain $A_V = -R_f / R_i$. The tuned circuit consists of L, C_1 and C_2 connected between the output and the input of the amplifier as shown in the figure (14.2). The output voltage V_O is applied across C_2 and the voltage across C_1 are feedback to the amplifier.



14.2 Colpitt's Oscillator.

It is assumed that the tuned circuit does not have any resistance. Its resonant frequency is given by the following condition that the total circuit offers zero closed loop impedance at its natural frequency.

i.e., $X_L + X_{C_1} + X_{C_2} = 0$

$$j\varpi L + \frac{1}{j\varpi C_1} + \frac{1}{j\varpi C_2} = 0 \qquad \ldots(14.1)$$

or $$j\varpi L = -\frac{1}{j\varpi}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \quad \text{or}$$

$$\varpi^2 = -\frac{1}{j^2 L}\left[\frac{1}{C_1} + \frac{1}{C_2}\right]$$

or $$\varpi_o^2 = \frac{1}{L}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) = \frac{1}{LC_v} \qquad \ldots (14.2)$$

or $$f_O = \frac{1}{2\pi\sqrt{LC_{eq}}} \text{ where } C_e = \frac{C_1 C_2}{C_1 + C_2} \qquad \ldots (14.3)$$

Let us now apply the Barkhausen's exiterion and calculate the feedback factor at this frequency. It is given by

$$|\beta^+| = \frac{V_f}{V_O} = \frac{V_f}{V_t} * \frac{V_t}{V_O} \qquad \ldots (14.4)$$

V_t is the tank circuit voltage given in the fig (14.2)

$$\frac{V_f}{V_t} = -\frac{1/J\varpi C_1}{1/J\varpi C_1 + 1/J\varpi C_2} \qquad \ldots (14.5)$$

multiplying both numerator and denominator by $j\ \varpi\ C_1\ C_2$

$$\frac{V_f}{V_t} = -\frac{C_2}{C_1 + C_2} \qquad \ldots (14.6)$$

and simplify,

$$\frac{V_t}{V_O} = \frac{1/j\varpi C_1 + 1/j\varpi C_2}{1/j\varpi C_2} \qquad \ldots (14.7)$$

multiplying both numerator and denominator by $(J\ \varpi\ C_1\ C_2)$

$$\frac{V_t}{V_O} = \frac{C_2 + C_1}{C_1} \qquad \ldots (14.8)$$

$$\therefore \beta = \frac{V_f}{V_O} = \frac{V_f}{V_t} * \frac{V_t}{V_O} = \frac{-C_2}{C_1 + C_2} * \frac{C_1 + C_2}{C_1} = \frac{-C_2}{C_1} \qquad \ldots (14.9)$$

The Gain of the amplifier $A = \frac{-R_f}{R_i}$ ... (14.10)

The minus sign in the above equation indicates the phase difference of 180^0 between V_f and V_t. Applying Barkhausen criterion, the loop gain is given by

$$|\beta A_v| = \left(\frac{-C_2}{C_1}\right)\left(\frac{-R_f}{R_i}\right) = 1 \equiv \frac{C_2 R_f}{C_1 R_i} \qquad \ldots (14.11)$$

or $$\frac{R_f}{R_i} = \frac{C_1}{C_2} \qquad \ldots (14.12)$$

is the condition for maintenance of oscillations. In practical oscillators C_1 is made variable and is adjusted to satisfy the above condition.

14.3 THE HARTLEY'S OSCILLATOR

The circuit diagram of the Hartley's oscillator is shown in Fig. 14.3. In this oscillator, tuned circuit consists of C, L_1 and L_2. The output voltage is connected across L_2 and the voltage across L_1 is the feedback voltage.

The tuned circuit offers zero closed loop impedance at its natural frequency given by

$$XL_1+XL_2+XC = 0$$

$$j\varpi L_1 + j\varpi L_2 + \frac{1}{j\varpi C} = 0$$

$$j\varpi (L_1+L_2) = -\frac{1}{j\varpi C}$$

$$\varpi^2 = \frac{1}{C(L_1+L_2)}$$

or $$\varpi = \frac{1}{\sqrt{C(L_1+L_2)}}$$

$$f = \frac{1}{2\pi\sqrt{C(L_1+L_2)}} = \frac{1}{2\pi\sqrt{CL_{eq}}} \quad \ldots (14.13)$$

where $L_{eq} = L_1+L_2$

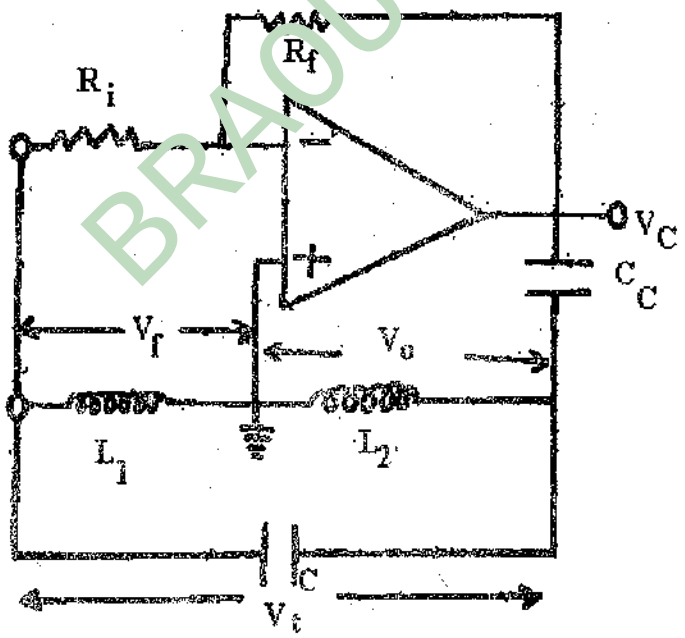


Fig. 14.3 Hartley Oscillator

At this frequency, the feedback factor is given by

$$\beta^+ = \frac{V_f}{V_o} = \frac{V_f}{V_t}\frac{V_t}{V_o} \quad \ldots (14.14)$$

$$\frac{V_t}{V_o} = \frac{j\varpi L_1 + j\varpi L_2}{j\varpi L_2} = \frac{L_1+L_2}{L_2} \quad \ldots (14.15)$$

and similarly

$$\frac{V_f}{V_i} = \frac{j\omega L_2}{j\omega L_1 + j\omega L_2} = -\frac{L_1}{L_1 + L_2} \qquad \ldots (14.16)$$

$$\beta^+ = -\left(\frac{L_1}{L_1 + L_2}\right)\left(\frac{L_1 + L_2}{L_2}\right) = -\frac{L_1}{L_2} \qquad \ldots (14.17)$$

the gain of the amplifier $A = \frac{-R_f}{R_i}$ ... (14.18)

Applying Barkhausen's condition, the loop again is given by

$$|\beta A_V| = \left(\frac{-L_1}{L_2}\right)\left(\frac{-R_f}{R_1}\right) = 1 = \frac{L_1 R_f}{L_2 R_i} \qquad \ldots (14.19)$$

We get

$$\frac{R_f}{R_i} = \frac{L_2}{L_1} \quad \text{i.e.,} \quad |A| = \left|\frac{1}{\beta}\right| \qquad \ldots (14.20)$$

This is the condition for maintenance of oscillations. In practical Hartley oscillators, a single inductance coil is used with tappings instead of separate L_1 and L_2.

14.4 SUMMARY

LC Oscillators produce higher frequencies than RC oscillators. Two such circuits are Colpitt's a Hartley's oscillators. Frequency of oscillation is determined by the Resonant frequency of the L, C combination in the Hartley's tank circuit.

14.5 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail

1. Explain how LC circuits can be used as frequency selective elements in radio frequency oscillators. Give the theory of the Hartley Oscillator.

2. Draw the circuit diagram of the Colpitt's oscillator and explain its working. Arrive at the maintenance equation

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14.7 GLOSSARY

Barkhausen criterion	:	Conditions to be satisfied by an amplifier arrangement to produce oscillations.
Oscillators	:	Circuits that generate waveforms of desired frequencies.
Phase-shift network	:	A circuit that introduces phase difference between its input and Output.

UNIT – 15 MULTIVIBRATORS

Contents

15.0 INTRODUCTION

A multivibrator is also known as a relaxation oscillator or Non sinusoidal oscillator; consisting of two stage RC coupled amplifier with the output of each stage coupled regeneratively to each other. The relative condition of each of the two stages are conduction in the first stage and cut off in the second stage or vice versa is termed as state of the multivibrator. The condition for the multivibrator is that it may remain indefinitely in the same state until the circuit is triggered by some external signal it is known as stable state. Multivibrators perform a variety of useful functions like generation of square waveforms, counting, frequency division, generation of time delays etc. The multivibrators can be classified into three categories.

1. Astable multivibrator or free running multivibrator
2. Monostable multivibrator or one shot multivibrator
3. Bistable multivibrator.

Astable Multivibrator

Astable multivibrator is a multivibrator in which neither state is stable. There are two temporary (quasistable) states. The circuit changes state continously from one quasi-stable state to another at regular time intervals without any triggering. This generates continous square waveform without any external signal.

Monostable Multivibrator

Monostable Multivibrator is also known as "**one shot multivibrator**". This has only one state. When a pulse is applied to the input circuit, the circuit state is changed abruptly to unstable state for a predetermined time after which the circuit returned to its original stable state automatically The circuit enables production of pulses of variable width at the required moment.

Bistable Multivibrator

Bistable Multivibrator is also known as "Flip - Flop". It has two stable states. Bistable circuit may stay in a particular state indefinitely and hence it can be used to store binary bit of information. When an external trigger is applied, the state of binary is

changed. At the occurrence of each triggering pulse, the circuit state changes abruptly from one state to another This is used as a digital memory device.

15.1 ASTABLE MULTIVIBRATOR

A free running multivibrator has no stable slates, but the circuit has two quasi-stable states, when transistor T_1 ON and transistor T_2 OFF and transistor T_1 OFF and transistor T_2 ON, and it makes periodic transitions between these states without any eternal triggering. Fig10.10(a) show the circuit diagram of an Astable multivibrator, and figure 10.10(b) gieven the output waveforms. The R_{L1} & R_{L2} are the collector resistance for transistors T_1 & T_2 respectively C_1 & C_2 are coupling capacitors, R_{B1} and R_{B2} provide on base current to the two transistors respectively during saturation region. Under symmetrical condition $R_{L1} = R_{L2}$: $R_{B1} = R_{B2}$ & $C_1 = C_2$, i.e., the components in one half of the circuit are considered to be equal to their components in the other half.

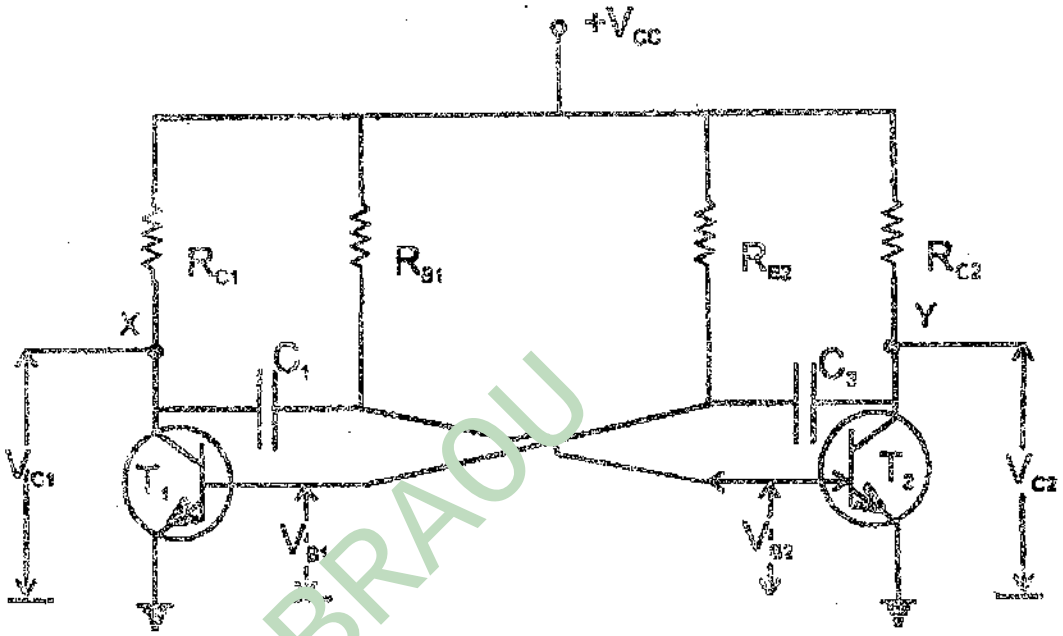

Fig15.1(a) Astable multivibrator

The operation of the circuit can be explained as follows

(i) When transistor T_1 is in saturation, the whole V_{CC} drops across R_{C1} i.e. $V_{CC}=I_C R_{C1}$, $V_{CC} = V_{C1} + I_C R_{C1}$ or $V_{C1} = V_{CC} - I_C R_{C1}$ show $V_{C1} = 0$(at point x) and hence the lower end of R_{C1} is at zero or ground potential.

(ii) Since the other end of $R_{C1}$is connected to the base B_2 of T_2 it is also at the ground potential. Hence I_{B2} is zero and, the transistor T_2 is cut-off i.e., it conducts no current. Hence, there is no voltage drop across R_{C2}, the supply potential and the end of R_{C2} is at potential V_{CC}.

(iii) When lower end of R_{C1} is at zero potential, the condenser C_1 start charging through R_{B1} towards V_{CC}.

(iv) When the voltage across C_1 rises to more than 0.7 volt, the transistor T_2 is forward biased and hence starts conducting. The transistor T_2 is soon driven to saturation.

(v) When transistor T_2 is in saturation position, the voltage V_{C2} becomes almost zero i.e., $V_{CC} = I_C R_{C2}$. We know $V_{CC} = V_{C2} + I_C R_{C2}$ or $V_{C2} = V_{CC} - I_C R_{C2} = 0$ i.e., the potential

at the lower end of R_{C2} decreases from V_{CC} to zero volt. This potential decrease is applied to the bases of transistor T_1 through C_2. Consequently T_1 is pulled out of saturation and is soon driven to cut-off.

(vi) In the cut-off position of T_1, the lower end of R_{C2} is at zero potential and hence the condenser C_2 starts charging through RB_2 to potential V_{CC}

(vii) When voltage across C_2 is more than 0.7 volt, the transistor T_1 is forward biased and starts conducting.

Thus the circuit switches automatically from cut-off to saturation and vice-versa

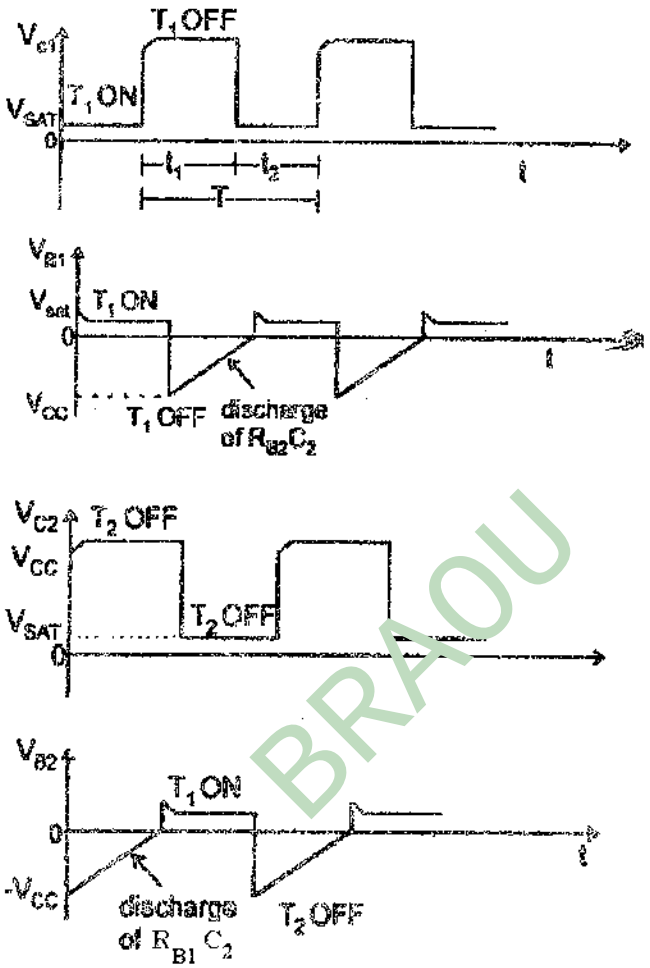

Figure 15.1(b) Output waveforms of Astable multivibrator Circuit conditions

15.2 FREQUENCY OF OSCILLATIONS

The frequency of oscillations can be calculated on the following way:

During the discharge of condenser C_2, the value of V_{B2} is given by

$$V_{B2} = V_{CC} - 2V_{CC}e^{(-t/R_{B1}C_1)} \qquad \ldots(15.1)$$

suppose $V_{B2} = 0$ & when the transistor is switched, then

$$0 = Vcc[1 - 2\,e^{-(t/R_{B1}C_1)}$$

$$\therefore e^{(-t/R_{B1}C_1)} = \tfrac{1}{2}$$

$$t = -R_{B1}C_1\log 2 = 0.694R_{B1} \bullet C_1 \qquad \ldots(15.2)$$

Thus at OFF time (t_2) for transistor T_2 or the ON time of transistor T_1 is given by

$$t_2 = 0.694\ R_{B1} \circ C_1 \qquad \ldots(15.3)$$

Similarly the OFF time (t_1) for transistor T_1 or the ON time of transistor T_2 is given by

$$t_1 = 0.694\ R_{B2} \circ C_2 \qquad \ldots(15.4)$$

The total time period $T = 0.694\ (R_{B1} \circ C_1 + R_{B2} \circ C_2)$ $\ldots(15.5)$

When $R_{B1} = R_{B2} = R$ and $C_1 = C_2 = C$, then total time period $T = 1.39\ RC$

The frequency of free running multivibrator is given by

$$f = \frac{1}{\text{total time period (T)}} = \frac{1}{1.39RC} = \frac{0.7}{RC} \qquad \ldots(15.6)$$

15.3 MONOSTABLE MULTIVIBRATOR

A monostable multivibrator has one stable state (i.e.,) permanent and other as temporary (i.e.,) quasi stable. When an external trigger is applied to the input, the multivibrator changes the state from stable (i.e.,) to quasi stable. It stays in quasi-stable state for a predetermined period after which the circuit returns to its original stable state automatically. Hence, it is also called One-Shot MultiVibrator.

A generalised circuit of a monostable multivibrator using active devices T_1 and T_2 is shown in figure 15.2(a).

Suppose that a external trigger is applied to X_2 and regenerative action takes place which drives T_2 to completely cut off. The voltage at Y_2 rises approximately to V_{CC}. Now T_1 comes in conduction. The device may be driven into saturation In this case a current I_1 flows in R_{C1} which causes a voltage drop $I_1 R_{C1}$ at Y_1 and thereby increasing the voltage across conductor 'C' which cannot change instantaneously The multivibrator is now in its quasi- stable state. The circuit will remain in this state only for a finite time because Y_2 is connected to V_{CC} through R_C. Now X_2 will rise in voltage.

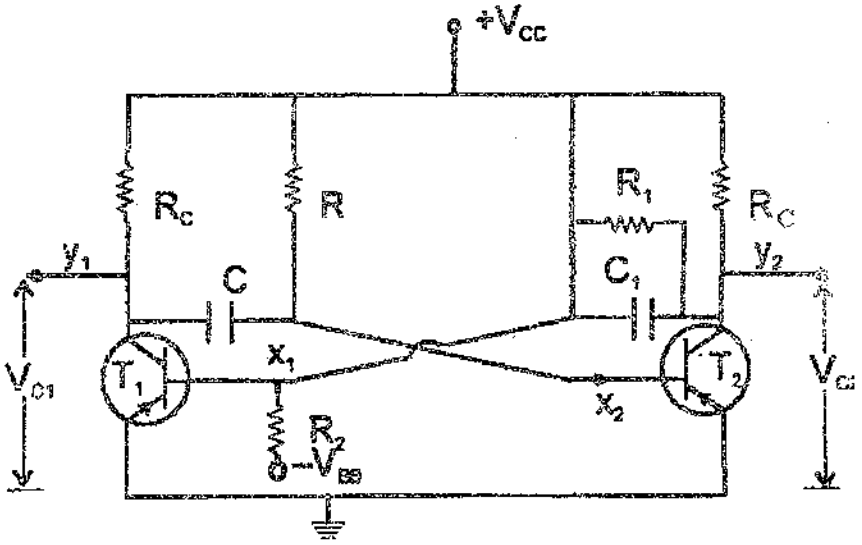

Figure 15.2(a) Collector coupled monostable multivibrator

When voltage across X_2 is equal to the cut in voltage T_2, a regenerative action takes place. This turns off and eventually returning the multivibrator to its stable state T_1 OFF and T_2 ON. A collector- coupled monostable circuit using NPN transistors is shown in figure 10.11. The triggering signal is applied at t = 0 and reverse transition across at t = T

15.4 THE QUASI-STABLE STATE

Let a negative trigger (short duration pulse) is applied toY_1 at t = 0. The change in potential at Y_1 is immediately transmitted to B_2 through canacitor C. Now the transistor T_2 is switched off, as the transistorT_2 switches off, the potential at Y_2 rises to almost the value V_{CC} from its stable value Vc_E(sat). This increases the potential at B_1 and the transistor T_1 comes into saturation. The potential at Y falls by $V_{CC} - V_{CE}$(sat).This change is communicated to B_2. All the above changes takes place due to regenerative feed back.

$$(V_{B2})_i = V_{BE(sat)} - (V_{CE} - V_{CE(sat)})$$

$$(V_{B2})_i = V_{BE(sat)} + V_{CE(sat)} + Vcc$$

At t = 0, transistor T_2 is cut off and the potential at B_2 rises exponentially with time due to charging of capacitor C. The potential V_{B2} starts rising towards +Vcc with a time constant RC. The instantaneous base voltage V_{B2} can be represented as

$$(V_{B2}) = (V_{B2}) + [(V_{B2})_i - (V_{B2})_f]e^{(-t/RC)}$$
$$(VB_2) = V_{CC} + [(V_{BE(sat)} + V_{CE(sat)} - 2VCC]e^{(-t/RC)} \quad \ldots(15.7)$$

The potential at the base of transistor T_2 does not rise to the maximum value because as soon as the potential rises to cut in voltage, T_2 is switched on due to regenerative feed back. The potential at the point Y_2 falls to its stable value $V_{CE(sat)}$.

The gate width of the output pulse is defined as the time interval between OFF and ON. In order to calculate the gate width we make use of $V_{B2} = V\gamma$ at t = T then we have

$$V_\gamma = V_{CC} + [V_{BE(sat)} + V_{CE(sat)} - 2V_{CC}]e^{-(T/RC)} \quad \ldots(15.8)$$

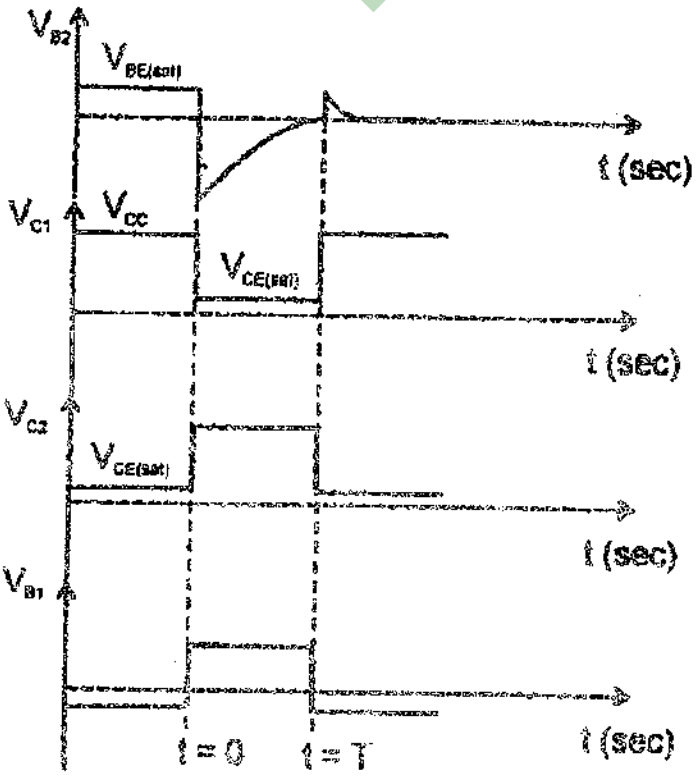

Figure 15.2(b) Waveforms of Collector coupled monostable multivibrator

$$V_\gamma - V_{CC} = [V_{BE(sat)} + V_{CE(sat)} - 2V_{CC}]e^{-(T/RC)}$$

Take antilog on both sides, and simplify we get

$$T = RC \log \frac{2V_{CC} - V_{BE(sat)} - V_{CE(sat)}}{V_{CC} - V_\gamma}$$

$$T = RC\left[\log 2 + \log\left(\frac{VCC - \{V_{BE(sat)} + V_{CE(sat)}\}/2}{V_{CC} - V_\gamma}\right)\right] \quad ...(15.9)$$

$$T = RC \log 2 + RC \log\left(\frac{VCC - \{V_{BE(sat)} + V_{CE(sat)}\}/2}{V_{CC} - V_\gamma}\right) \quad ...(15.10)$$

At room temperature,

$$VBE\ (sat) + VCE(sat) = 2Vg$$

$$T = RClOg2 + RClogl = RClog'2 \quad ...(15.11)$$

$$T = 0.69\ RC$$

As soon as T_2 begin to conduct, a regenerative action makes T_1 OFF and T_2 ON then the circuit remains in stable state until another trigger is applied.

15.5 BISTABLE MULTIVIBRATOR

A Bistable Multivibrator means, it has two stable states. The circuit can stay in any one of the stable states indefinitely and makes an abrupt transition from one state to other state when the triggered. A Bistable Multivibrator is used for the performance of many digital operations such as counting and storing the binary information (i.e., used as flip flops or memories).

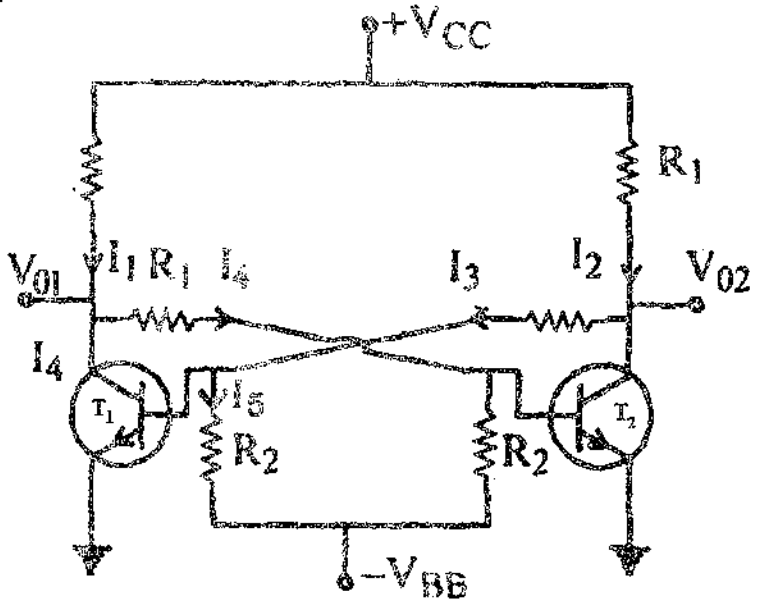

Figure 15.3(a) Bistable Multivibrator

The circuit diagram of Bistable Emitter vibration is shown in Fig. 15.3(a). The amplifiers are coupled in such a way that one transistor is in ON state (saturation) and other transistor is in OFF state (cut off region). The transistor is changing from one state to other state by n applying the triggering pulse.

In this the output of one amplifier is feed back to the Input of second amplifier. Each amplifier produces a phase shift of 180^0 and hence the amplifiers provided with positive feedback at all frequencies. Because of the symmetry the current and voltages of the above said circuit is equal. For a momentary a trigger signal is applied at the collector terminal of T_1 then, the current I_1 in transistor is decrease hence the potential at collector terminal of T_1 increase. This will more forward biases the transistor T_2 hence it enters into saturation region result in which I_2 in transistor T_2 increases, hence the collector potential of T_2 reduced to zero, it is supplied to the base of transistor T_1, so the transistor T_1 is entered in cutoff region (i.e., OFF state). This condition is remains in the same state until the next trigger pulse is applied, then T_1 entering into ON state T_2 enters in OFF state.

The two stable states of the bistable multivibrator are

(i) T_1 OFF and T_2ON

(ii) T_2 OFF and T_1 ON

The different values of current and voltages of Bistable Multivibrator when T_1 OFF and T_2 ON

15.6 SCHMITT TRIGGER

The above figure 15.4 shows the circuit of a schmitt triger. The Schmitt trigger is used for wave shaping circuits. It can be used for generation of a square wave from a sine-wave input. The circuit has two opposite operating states as in all multivibrator circuits. Here the trigger signal is a slowly varying AC voltage. The schmitt trigger is level sensitive and switches the output state at two distinct trigger levels. One of the triggering level is the -lower-trigger level and other is the upper-trigger level.

The circuit consists of two identical transistors T_1 and T_2 coupled through an emitter R_E. The resistors R_1 and R_2 form a voltage divider across the V_{CC} supply and ground. These resistors provide a small forward bias on the base of transistor T_2. The operation of the circuit may be explained as follows:

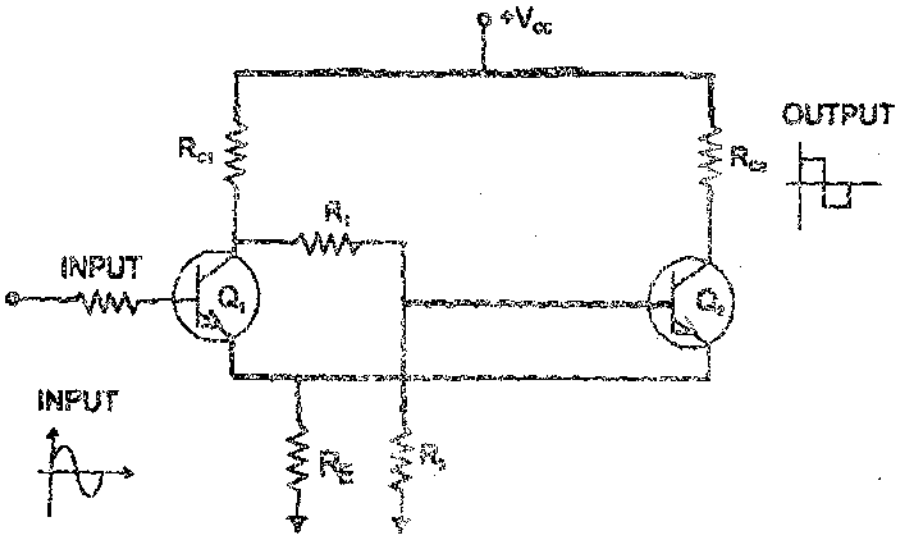

Figure 15.4(a) Schmitt Trigger

Let there be initially no signal at the input. Now when power supply is switched on, the transistor T2 starts conducting. The current through R_E produces voltage drop across it. The voltage drop acts as a reverse bias across the emitter base junction of transistor T_1 due to which it is cut off. So the voltage at its collector rises to V_{CC}. This rising voltage is coupled to the base of T_2 through R_1, which increases the forward bias at the base of T_2 and so drives it into saturation. At this instant, the collector voltage levels are $V_{C1} = V_{CC}$ and $V_{C2} = V_{CE\,(sat)}$.

Now, suppose an AC signal is applied to the input nothing happens until Upper Trigger Level (UTL) is reached. But once the input voltage is more than UTL then transistor, T_1 conducts. The point at which it occurs is called "Upper Trigger Point (U.T.P)". As T_1 conducts, its collector voltage falls below V_{CC}. This fall is coupled through resistor R_1 to the base of T_2, which reduces its forward bias, and T_2 enters into off state This results in voltage drop across R_E so the reverse bias of T_1 is reduced and it conducts more. As T_1 conducts more heavily, its collector current further reduces due to which the transistor T2 conducts near cut off. This process continues till T_2 is driven to cut off and T_1 to saturation.

The transistor T_1 will conduct till the input voltage falls below the Lower Trigger Level (L.T.L). When the input voltage becomes to L.T.L, the emitter base junction of transistor Ti is reverse biased. Hence, the collector voltage increases towards V_{CC}. This rising voltage increases the forward bias across T_2, due to which it conducts. The point at which T_2 starts conducting, is called Lower-Trigger Point (L.T.P). Soon the transistor T_2 is driven to saturation and T_1 is cut off. The collector voltage levels at this instant are $V_{C1} = V_{CC}$ & $V_{C2} = V_{CE(sat)}$. No change in state will occur during the negative half cycle of the input voltage.

From the above discussion, it is clear that output of a schmitt trigger is a positive going pulse, whose width depends upon the time during transistor T_1 is conducting. The conduction

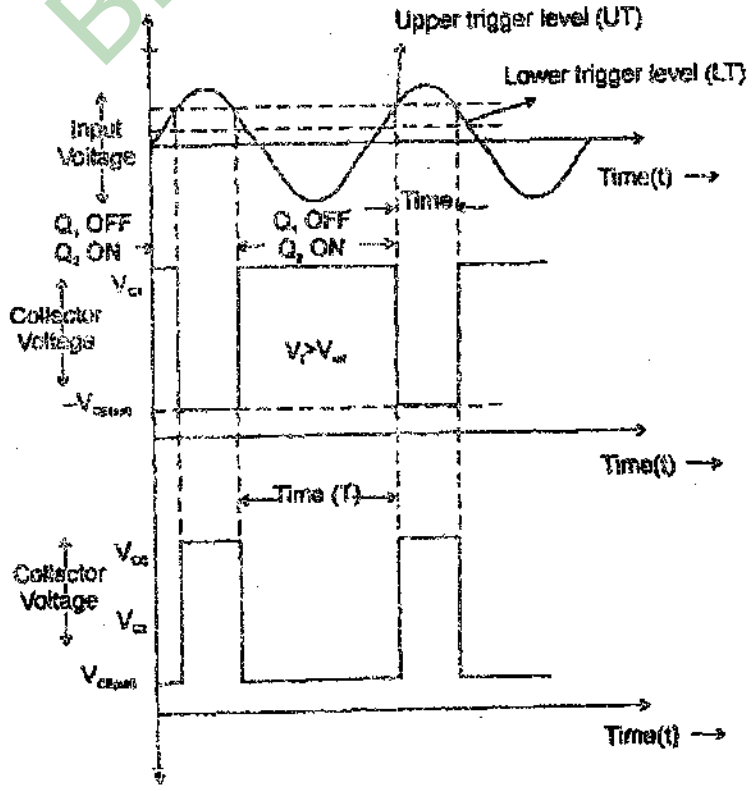

Figure 15.4(b) Waveforms of Schmitt Trigger

15.7 SUMMARY

The non-sinusoidal oscillator like Atable MV, provide. It necessary for timing signals. Monostable can be used for frequency division or delay producing circuit. Schmitt Trigger is useful as a squaring circuit i.e., it converts any given non-square wave inputs like a (sine or ramp) into square wave.

15.8 MODEL EXAMINATION QUESTIONS

I. Answer the following questions detail.

1. Define the term astable multivibrator.
2. Define the term monostable multivibrator.
3. What is the usefulness of a monostable multivibrator?
4. Name the application of a Schmitt Trigger Circuit.

II. Answer the following questions Briefly.

1. Explain the working of an astable multivibrator and derive expression for its frequency of oscillators.
2. Give the design of a monostable multivibrator. Derive expression for the time period of the quasi-stable state.
3. Give the circuit diagram of a Bistable multivibrator and explain its working.

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BLOCK – V

POWER SUPPLIES AND REGULATION

UNIT 16: RECTIFIERS AND FILTERS

Contents:

16.0 AIMS AND OBJECTIVES

This unit introduces you to the process of converting A.C. into D.C. For this purpose we are going to study

1) the unilateral behavior of a diode and how it can be used for rectification (Conversion of AC into DC)
2) different types of rectifiers
3) the method of eliminating ripple using filters and
4) the circuit for voltage multiplication

After going through this unit you will be able to explain

1) the process of rectification
2) the need for filtering and
3) the process of voltage multiplication

16.1 INTRODUCTION

Electronic instruments in general need D.C. power supply for biasing. A convenient method of obtaining D.C. power is to rectify A.C. power line voltage using diodes. The rectifier output is a pulsating DC voltage but not a pure DC voltage. When smoothened by a filter an yields approximately steady DC voltage over which a small ripple voltage is superposed.

High voltages can be obtained by employing voltage multiplier circuits in which capacitors are used to store the energy.

16.2 THE PROCESS OF RECTIFICATION

Rectification is the process of converting alternating current into unidirectional but pulsating' current. It is illustrated in Fig. 16.1. In fig. 16.1b only one half a cycle of the wave is rectified.

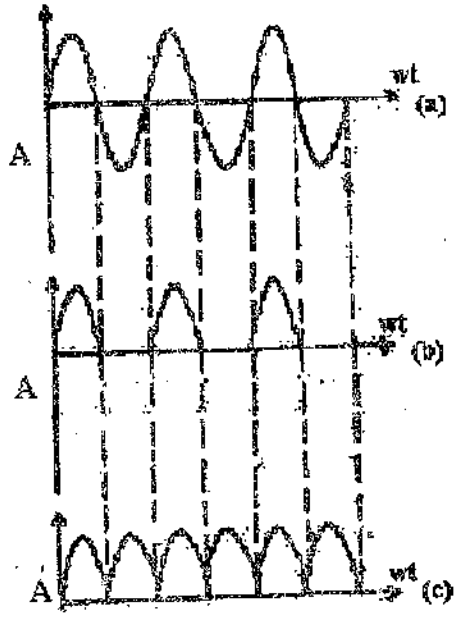


Fig 16.1 Rectification A-amplitude
a- Input ac wave
b- Half wave rectification
c- Full wave rectification

Hence it is called half-wave rectification. Full-wave rectification makes use of both the half cycles of the wave. In this process, we make use of the unilateral conduction characteristic of the diode i.e. low resistance in the forward direction and high resistance in the reverse direction. Half wave rectifiers use only one diode while full-wave rectifiers use two or four diodes. The pulsations at the output of the rectifier are removed or smoothened by frequency selective networks, called filters. Filter circuits use the energy storage capabilities of inductors and capacitors to smooth out the pulsations and to provide steady currents. The combination of the ac source normally a transformer, rectifier, and a filter constitute a simple power supply. However power supplies used for for sophisticated applications incorporate regulators also. The regulators maintain the output for DC voltage constant irrespective of the changes in the AC mains voltage or the load currents.

16.3 HALF-WAVE RECTIFIER

An ideal diode should allow current conduction (flow) freely in the forward direction and prevent current conduction (flow) in the reverse direction. That is, they offer zero resistance in the forward direction and infinite resistance in the reverse direction. Real diodes behave differently. Semiconductor diodes present a small but appreciable resistance in the forward direction and large but finite resistance in the reverse direction. Hence, there will be a small voltage drop in the forward direction and a small minority charge current flow in the reverse direction. However, for purposes of understanding the working of a rectifier, we may safely assume the ideal characteristics.

Fig. 16.2 shows an elementary half–wave rectifier. It consists of a Semi-conducting diode in series with an ac source and a load resistance R_L. When the polarity of the ac source is in the forward direction (when it lies between 0 and π), the diode conducts and produces

a current pulse.

$$I = \frac{V}{R_L} = \frac{V_m Sin\varpi\ t}{R_L} \quad \text{for } 0 \le \varpi t \le \pi \qquad \ldots (16.1)$$

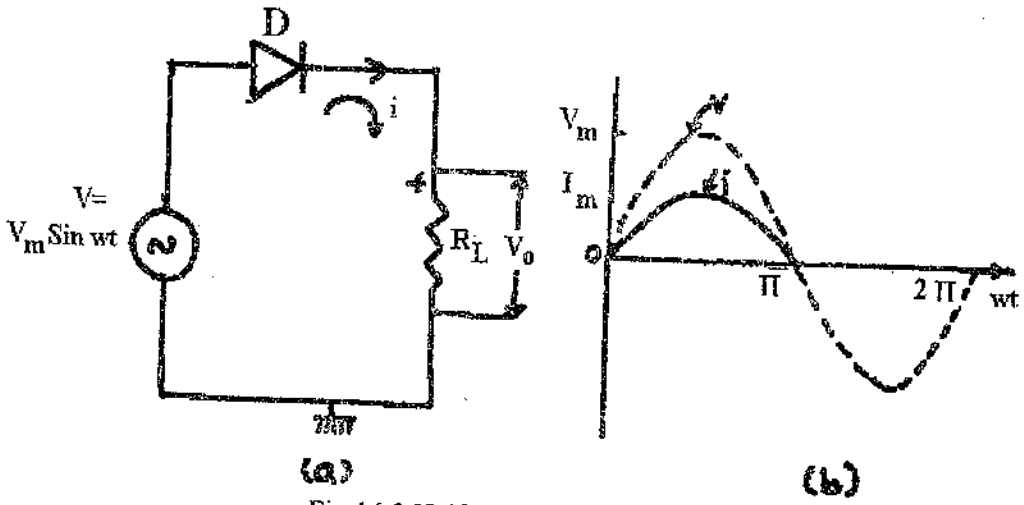


Fig 16.2 Half wave Rectification
(a) Circuit (b) wave form
D-diodes, v- input voltage, i-current
Vo = Output Voltage

During the reverse half-cycle, the current is zero i.e.

$$I = 0 \text{ for } \pi \le \varpi\ t \le 2\pi \qquad \ldots (16.2)$$

The output current is therefore a succession of positive half cycles of sine waves as shown in Fig. 16.2. b. The average value of the load current is given by

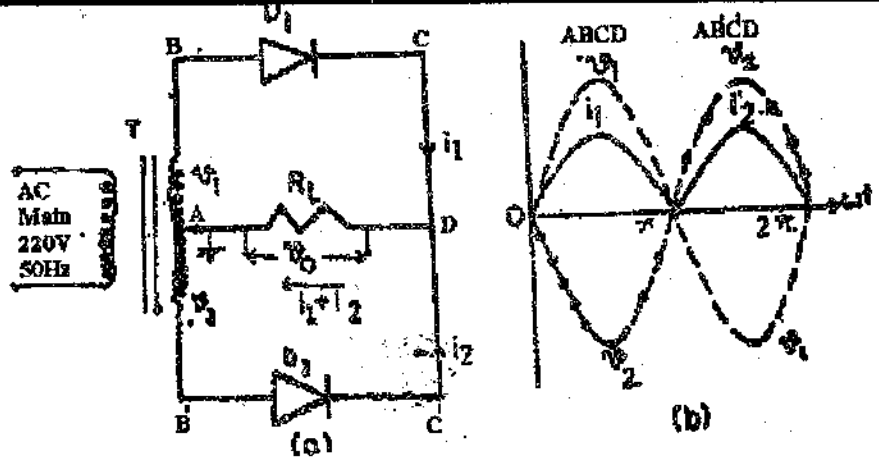
$$I_{dc} = \frac{V_m}{\pi R_L} \qquad \ldots (16.3)$$

Where V_m and I_m are the peak values of the rectified DC voltage and DC current respectively

16.4 FULL - WAVE RECTIFIER

A. Using Centre Tapped Transformer and two Diodes:

In the half-wave rectifier discussed above, only one of the half cycles, of the input wave are allowed to pass current. With a minor modification in the circuit both the halve cycles can be rectified using the circuits shown in Figs. 16.3 and 16.4. In the arrangement shown in Fig 16.3 we use two diodes. The center-tapped transformer provides the necessary ac voltages. When V_1 positive diode D_1 is forward biased and conducts during one half of the input cycle while D_2 is reverse biased and does not conduct. When V_2 is positive during the other half of the cycle, diode D_2 is forward biased and conducts while D_1 is reverse biased. The output voltage and current waveforms are shown in Fig. 16.3. b. The current flows



Fig, 16.3 Full wave rectifications
(a) Circuit (b) Wave forms

is in the same direction in the load resistance during both the halves of the input cycle. The dc component is twice as large as in the half-wave rectifier.

$$I_{DC} = \frac{2V_m}{\pi R_L} \quad \ldots (16.4)$$

B. Bridge Rectifier:

Another arrangement for full-wave rectification is shown in Fig. 16.4. It makes use of four diodes arranged in the four arms of the bridge, when the transformer voltage polarity is such that the point A is positive with respect to point D, diodes D_1, and D_3, conduct and the current

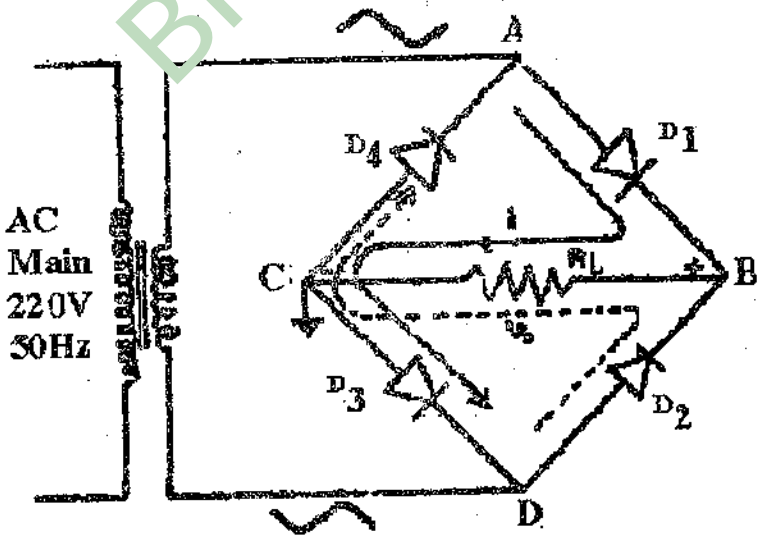


Fig. 16.4 Bridge rectifier
(a) Circuit

takes the path ABCD through load R_L. It results in a half sine wave of current flow. When the voltage reverses its polarity, diodes D_2 and D_4 conduct and the current takes the path DBCA through load R_L. However, the current through the load resistor-R_L always takes the same path i.e. from B to C. As mentioned earlier, the DC component is given by equation (16.4).

The full-wave rectifier circuit of Fig.16.3 uses a comparatively more expensive and bulky centre tapped transformer while the bridge rectifier circuit of Fig. 16.4 using four

diodes is available. It is convenient to use the bridge rectifier. It is inexpensive.

16.5 NEED FOR FILTERS

Rectification is meant to obtain direct current, but the output waveforms of the circuits described above contain large alternating current components know harmonies along with the DC component. For example, analysis of the output waveform of the full-wave rectifier shows that it is given by

$$V_o = \left(\frac{2V_m}{\pi}\right) - \left(\frac{4V_m}{3\pi}\right)\text{Cos}(2\varpi)\,t - \left(\frac{4V_m}{35\pi}\right)\text{Cos}(4\,\varpi)\,\ldots\ldots\ldots\text{etc.}\ \ldots\ (16.5)$$

The first term is a constant and represents the DC component. The second term is a second harmonic of relative magnitude 2/3 and frequency 2ϖ. The succeeding higher harmonic terms are smaller. Hence, for purposes of analysis we may consider up to the second harmonic term and neglect the higher harmonic terms containing 4ϖ t and 6ϖ t etc. It is clear from the above, that the output of a full-wave rectifier consists of a DC term and second harmonic term. In order to obtain a pure DC voltage, it is required to remove the second harmonic term. These low pass filters are more efficient in removing higher order harmonic components.

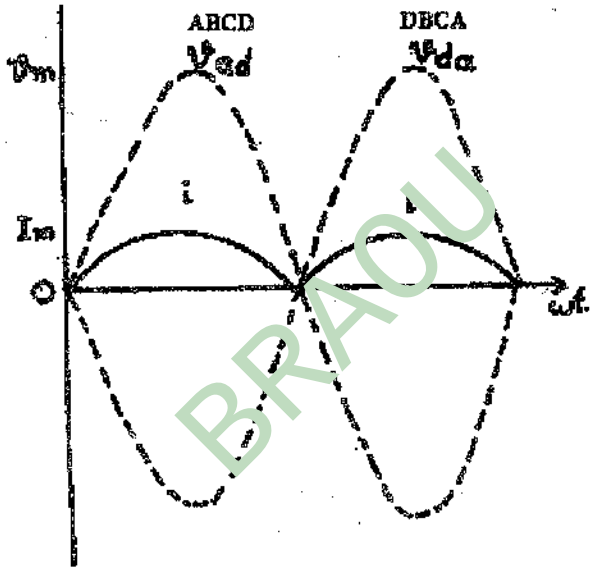


Fig. 16.4 (b) Wave forms

16.6 FILTERS

(a) Capacitor filter:

The simplest filter circuit consists of a capacitor connected in parallel with the load resistance R_L of a bridge rectifier as shown in Fig. 16.5. The capacitor gets charged

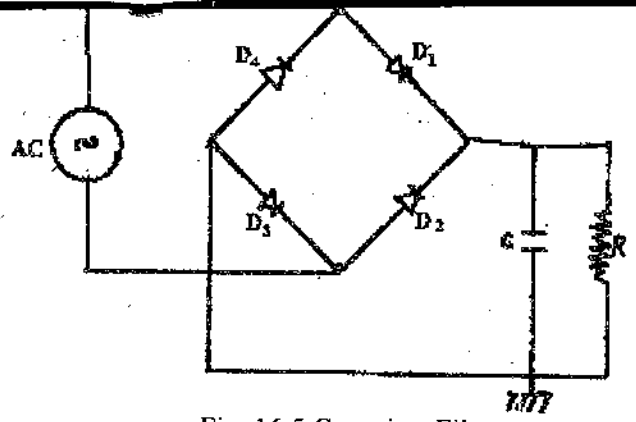


Fig. 16.5 Capacitor Filter
(a) Bridge circuit with Capacitor filter

to the peak value V_m of the rectified voltage in a short interval of time. It begins to discharge through R_L after the rectified voltage decreases from the peak value. The diode conducts during the period when the capacitor is getting charged. The rate of discharge depends upon the relative values of the time constant RC and the time period T of the reflected DC pulses.

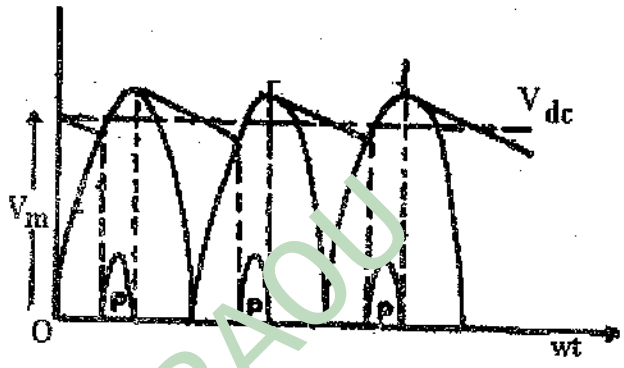


Fig. 16.5(b) wave forms
P -Conduction period of the diodes
T -Time period of the pulse

The waveform of the voltage across the capacitor can be taken as triangular (if R_L << T). The decrease in the capacitor voltage during the time period T is $\left[\frac{V_m T}{CR_L}\right]$. The DC output voltage is given by

$$V_{DC} = V_m - \frac{V_m T}{4CR_L}$$

$$= V_m - \frac{I_{DC}}{4fC} \text{ where } I_{DC} = \frac{V_m}{R_L} \quad \text{and} \quad T = \frac{1}{f} \quad \ldots (16.6)$$

The peak-to-peak value of the ac component, called ripple, is $\left[\frac{V_{DC}}{CR_L}\right]$ and the peak value is $\left[\frac{V_{DC}}{2CR_L}\right]$. The rms value of the triangular wave is equal to $(1/\sqrt{3})$ of its peak value. Hence the rms value of the ripple voltage is

$$V_{rms} = \frac{V_{DC}}{4\sqrt{3}fCR_L} \quad \ldots (16.7)$$

The-ratio of the rms value of the ripple voltage and the dc voltage is called the ripple factor r. For a power supply to be effective, it is necessary to minimise r. The ripple factor for the simple capacitance filter is given by

$$r = \frac{V_{rms}}{V_{DC}} = \frac{1}{4\sqrt{3}fCR_L} \qquad \ldots (16.8)$$

(b) L - Section Filter:

Another filter that is commonly used is shown in Fig. 16.6. The rectified voltage containing

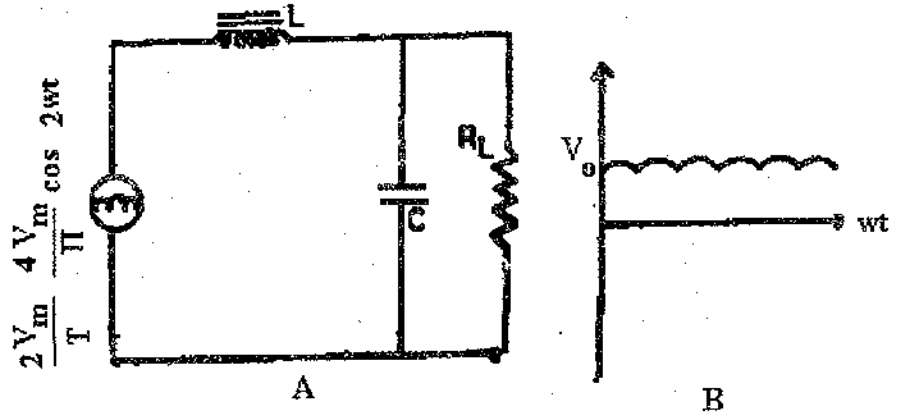


fig. 16.6 L-Section filter
(a) Circuit (b) Output wave form
Vo - Output Voltage

both the DC and AC components is applied to the series combination of L and C. The magnitude of L and C is assumed that or $X_C << R$ and $X_L >> X_C$. Under such conditions the AC current through L - C combination is decided entirely by the inductive reactance ϖL. The amplitude of the current is given by

$$I_m = \frac{4V_m}{3\pi} \times \frac{1}{\varpi L} = \frac{4V_m}{3\pi\varpi L} \qquad \ldots (16.9)$$

The voltage across the capacitance is given by

$$V_{rms} = IX_C = \frac{4V_m}{\sqrt{2}(3\pi)\varpi^2 LC} \qquad \ldots(16.10)$$

$$= \frac{2\sqrt{2}}{3\pi}\frac{4V_m}{\varpi^2 LC}$$

An ideal inductor offers zero resistance and an ideal capacitor offers infinite resistance to de. Hence the dc output voltage is given by

$$V_{DC} = \frac{2V_m}{\Pi} \qquad \ldots(16.11)$$

The ripple factor of the L-section filter is given by

$$r = \frac{V_{rms}}{V_{DC}} = \frac{\sqrt{2}}{3}\frac{1}{\varpi^2 LC} \qquad \ldots(16.12)$$

(c) π - Section Filter

The π section filter is shown in Fig. 16.7 it can be thought ofas a simple capacitor filter followed by an L-section filter. An ideal inductor does not obstruct DC and an ideal capacitor does not conduct DC. As such the L-C filter does not change DC voltage applied to it. Hence, the DC output voltage of this filter will be the same as that of the capacitor filter. It is expressed by equation (16.6).

$$V_{DC} = V_m - \frac{I_{DC}}{4fe}$$

The ripple voltage across the capacitor filter is expressed by equation (16.7). Assuming that this acts as input to the L-section filter, we have for ripple voltage of the - Π section filter

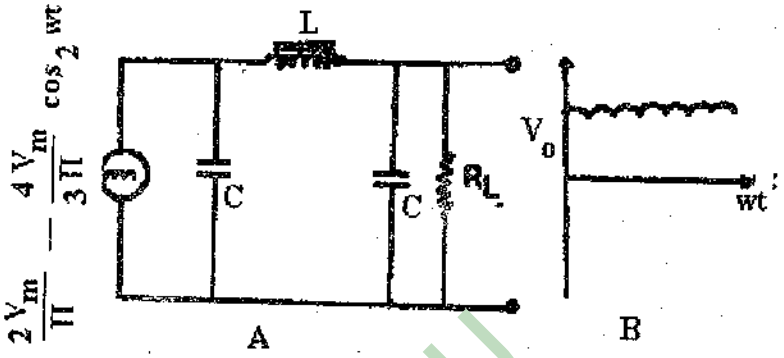


Fig. 16.7 Π - Section Filter
(a) Circuit (b) Wave form

$$V_{rms} = \frac{V_{DC}}{2\sqrt{3}fCR_L}\cdot\frac{1}{\omega^2 LC} = \frac{\pi \cdot V_{DC}}{(2\pi f)\sqrt{3}CR_L}\cdot\frac{1}{\omega^2 LC} \quad ...(16.13)$$

$$V_{rms} = \frac{\pi}{\sqrt{3}}\frac{V_{DC}}{R_L\omega^3C^2L}$$

The ripple factor is given by

$$r = \frac{V_{rms}}{V_{DC}} = \frac{\pi}{\sqrt{3}} = \frac{1}{R_L\omega^3C^2L} \quad ...(16.14)$$

16.7 FILTER CHARACTERISTICS

The variation of the DC output voltage with load current I_{DC} of a power supply with L and π section filters is shown in Fig. 16.8. As indicated by equation (16.6) the output voltage of the π -section filter decreases lineally with the load current $I_{DC}=I_L$ In practice the L-section confirms to this behavior at appreciably large load currents. For low load currents, the inductor becomes ineffective and the voltage drop across the inductor increases rapidly i.e. it behaves as a capacitor filter. Hence, the DC output voltage decreases rapid at low load currents.

According to equation (16.11), the DC output voltage of a power supply with L-section

filter should be independent of the load current.

L-section filters are used in applications where wide variations of load currents are expected. π -Section filters are used in situations where limited variations in load currents are expected.

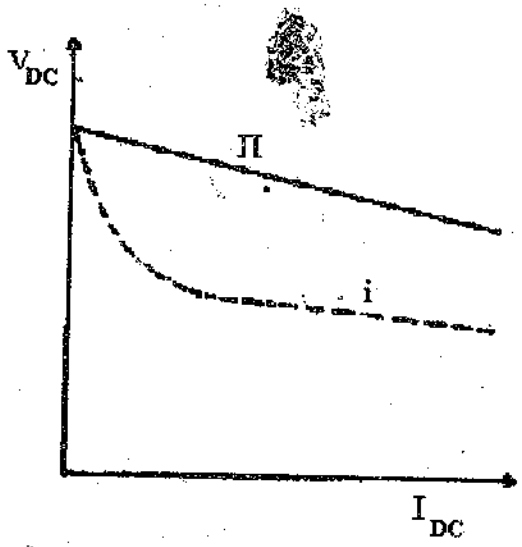


Fig. 16.8 Filter chameteristics-Variation of output Voltage $V_{DC}$with load Current
$I_{DC}=I_L$ -Load Current

16.8 VOLTAGE MULTIPLICATION

In certain applications we need high voltages, which need to deliver low currents. Voltage multipliers provide such high voltages.

Fig. 16.9 shows a circuit that provides a dc voltage having a magnitude equal to twice the peak value of the alternating input voltage. In the circuit, each of the capacitors C_1 and C_2, is charged to nearly the peak value of the input voltage during successive half cycles. The two capacitors are connected in series across the output terminals. If appreciable current is not drawn by R_L, the output voltage will be the sum of the voltages across the capacitors. A third capacitor C_3 is connected parallel to C_1 and C_2 such that that total DC voltage $V_{DC}+V_{DC} = 2\ V_{DC}$ is applied across it .This capacitor further reduces ripple voltages.

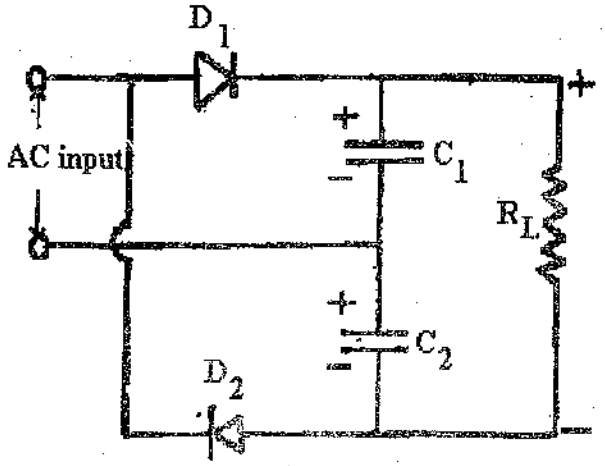


Fig. 16.9 Voltage doubler

Circuits based on similar principles may be designed to furnish output voltages that

integral multiples of the input peak voltage.

16.9 SUMMARY

Rectifiers convert AC voltage into DC voltage. Filter circuits remove the pulsations (or the ripple voltages) superposed over the DC output. High voltages can be obtained using voltage Multipliers.

16.10 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail

1. Draw the circuit diagram of a full wave rectifiers with π - section filters and explain its working.
2. Discuss the action of different filters.

II. Answer the following questions briefly.

1. Compare the full wave rectifiers with the half wave-rectifier.
2. Sketch the circuit of a bridge rectifier and explain its working.
3. Show that the ripple factor for the unfiltered full wave rectifier is 0.48.
4. Discuss the action of the π - section filters.
5. Discuss the action of the L- section filter

III. Solve the following problems.

1. Calculate the ripple factor of an L section filter consisting of 10H choke and 8 μ F capacitor used with a full wave rectifiers [Ans : 0.015]

2. The input to a π section filter is a full wave rectifier voltage with a 50V peak value. The load resistance resistance is 1k Ω. An 8H inductor is available. Determine the capacitors needed to produce a ripple factor of 0.001 (Assume $C_1 = C_2 = C$) [Ans : 30.2 μF)

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UNIT -17: VOLTAGE REGULATION

Contents:

17.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

(1) Voltage regulators, designed to maintain the output voltage constant

(2) Different types of regulators namely zener regulator and electronic regulator, switch mode regulator etc. are available for voltage regulations.

After going through this unit you will be able to discuss

1) The need for voltage regulation

2) Use of zener diode as a voltage regulator

3) Working of an electronic voltage regulator and calculate the percentage regulation.

4) IC regulators

5) Switch Mode Regulator

17.1 INTRODUCTION

Simple filters discussed in the previous unit cannot prevent load voltage variations due to fluctuations in the AC mains voltage and fluctuations in load current. The constant voltage drop across the reverse biased zener diode when operated in the breakdown region is made use of in the design of a zener voltage regulator (Shunt Resistor).

A transistor is used as a voltage controlled resister in series with the power supply and load in electronic regulator. The series voltage regulator offers higher regulation without much wastage of power in the regulator.

17.2 NEED FOR VOLTAGE REGULATION

The voltage across the load connected to a power supply may vary due to the following reasons.

(a) Cyclical variations in the rectifier output
(b) Fluctuations in the AC mains supply voltage (220 V, 50 Hz)
(c) Changes in the load current.

Filters can only minimise but cannot eliminate output voltage variations due to fluctuations in the AC mains supply voltage and due to variations in load current. However, electronic voltage regulators can efficiently maintain the rated output voltages in-spite of variations in mains supply voltage and the load current. They also serve as filters to certain extent.

17.3 REGULATOR CHARACTERISTCS

No regulator provides perfect regulation. Typical characteristics of an ideal and a real power supplies are shown in Fig. 17.1. The output voltage from any real power supply decreases with increasing load current as shown in the figure.

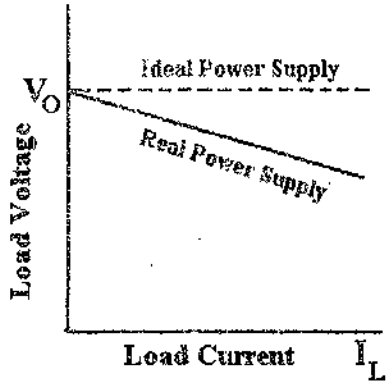

Fig 17.1 Variation of the output voltage Vo of a power supply with load current I_L Ideal regulation; TC-Typical characteristic Voc -open circuit voltage; V_L -Voltage under load

The amount of regulation provided by the regulator is indicated by, the percentage of regulation. It is given by

$$\% \text{ regulation} = \frac{V_{OL} - V_L}{V_L} X100\% \qquad ...(17.1)$$

where

V_{OL} = output voltage under no load condition
V_L = output voltage under load

It can be seen from Equ. 17.1 that the percentage regulation gives magnitude of deviation from the constant output voltage required. Hence, smaller the magnitude of %regulation better will be the constancy of the output voltage.

The voltage under any particular load current I_L may be expressed as

$$V_L = I_L R_L \qquad ...(17.2)$$

where R_L is the load resistance. We define the output resistance of the regulator as

$$R_O = \frac{V_{OC} - V_L}{I_L} \qquad ...(17.3)$$

Therefore combining equations (17.1), (17.2), (17.3) we obtain

$$\% \text{ regulation} = \frac{R_O}{R_L} X100\% \qquad ...(17.4)$$

For any given load current, regulation improves (% regulation decreases) as the output resistance or internal impedance of the regulator decreases. Hence a good regulator should have low internal impedance

17.4 ZENER REGULATOR – SHUNT REGULATOR

A simple shunt regulator using Zener diode is shown in Fig. 17.2. Since the Zener diode is connected in parallel with the load, the circuit is known as shunt Regulator. It consists, of a current limiting resistance R_S connected in series with the Zener diode of breakdown voltage V_Z. The load R_L is connected across the diode. The unregulated DC voltage V_i is chosen to be greater than the Zener breakdown voltage to ensure that the Zener operates in the reverse break down region. The unregulated DC power supply reverse biases the Zener diode. Vi should be chosen to be grater than Vz. The operation is based on the fact that when the Zener is operated in the breakdown region, the voltage drop across the Zener remains substantially constant over wide of current range. This property is made use of in the design of the Zener voltage regulator.

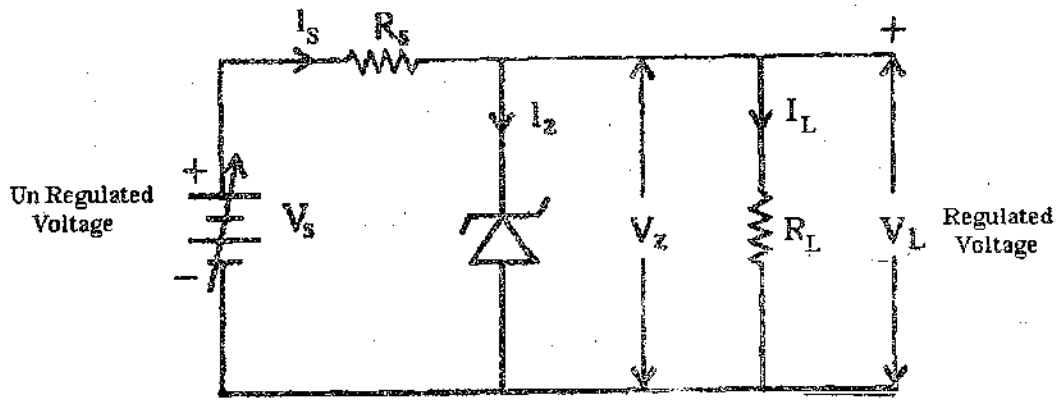

Fig. 17.2 Zener Voltage Regulator

Large changes in the load current are followed by small changes in the Zener voltage due to its low internal impedance. The large variation in the currents flowing through R_S produce voltage drops across it that counteracts and compensate for the changes in the output voltage produced due to variations in V_i and I_2.

In Fig. 17.2, if I_i be the current drawn from the source, and I_Z and I_L are the currents through the Zener diode and the load resistance respectively, we have (according to Kirchhoff's laws)

$$I_i = I_Z + I_L \quad \ldots (17.5)$$

$$V_O = V_i - I_i R_S \text{ or } R_S = \frac{V_i - V_O}{I_i} = \frac{V_i - V_Z}{I_i} \quad \ldots (17.6)$$

$$\text{Since } V_O = I_L R_L = V_Z \quad \ldots (17.7)$$

Let us consider the situation when V_i remains constant and load resistance R_L varies. Since the voltage drop across the Zener remains substantially constant, the output voltage $V_O = V_Z$ tends to remain constant. Since the total current drawn from the unregulated power supply is constant, there is no charge in I_i. Hence $dI_i = 0$ and differentiating to equation (17.5)

$$dI_i = 0 = dI_Z + dI_L \quad \ldots (17.8)$$

or

$$dI_Z = -dI_L \quad \ldots (17.9)$$

Thus, when the load resistance increases with V_i remaining constant, the current I_L decreases and the current Iz increases by the same magnitude so that the total current I_i remains constant.

If R_L remains constant and V_i varies. We have according to equation (17.6)

$$dV_O = 0 = dV_i - dI_i R_S$$

$$dV_i = R_S dI_i \quad \ldots (17.10)$$

from equation (17.9)

$$dI_L = 0 \quad \ldots (17.11)$$

and from equation (17.10)

$$dI_i = dI_Z$$

That is, when the DC supply voltage is altered under constant load R_L, the current I_i and the Zener current I_Z change equally to keep the load current constant.

Worked out example:

In a Zener regulator, the unregulated DC input is 10 volts and the Zener voltage is 5 volts. The maximum Zener current (I_Z) = 20 mA. Determine the value of R_S If a load resistance (R_L) of 2 kΩ is connected; calculate the load current and the Zener current.

Ans: The Zener current is maximum when the load resistance R is infinite, Hence

$$R_S = \frac{V_i - V_Z}{I_i} = \frac{10 - 5}{20x10^{-3}} = 250\Omega$$

The current through the load resistance of 2k is

$$I_L = \frac{V_O}{R_L} = \frac{5}{2X10^3} = 2.5mA$$

The Zerer current is

$I_Z = I - I_L = 20 - 2.5 = 17.5$ mA

17.5 ELECTRONIC REGULATOR – SERIES REGULATOR

Voltage regulators with better regulation than that is possible with simple Zener regulator may be designed using electronic control systems. The output voltage of such a regulator circuit is controlled by introducing a power transistor Q in series with the unregulated power supply and the load resistance R_L as shown in Fig. 17.3. The transistor Q is known as series pass transistor whose internal impedance and hence the voltage drop across it can be varied to oppose the changes in the output voltage. The transistor Q acts as a variable resistor in series with the load resistor R_L

The collector to emitter voltage drop across the series pass transistor is given by

$$V_{CE} = V_i - V_L \qquad \ldots (17.10)$$

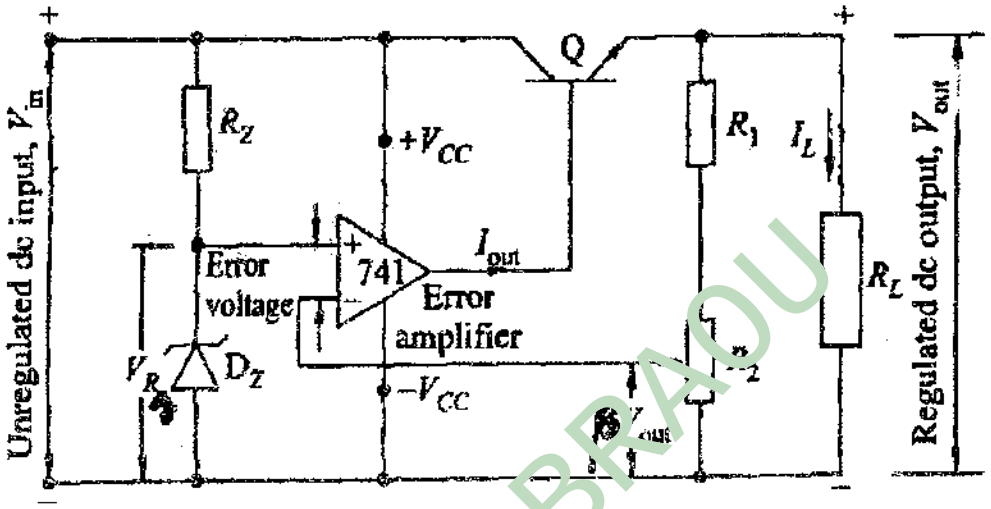

Fig. 17.3 Electronic Voltage Regulator
R_S - Series resistor to limit Zener current

A part of the load voltage (βV_L) is sampled and fed back to the inverting input of the op amp via the $R_1 - R_2$ potential divider network. The feedback factor β is given by

$$\beta = \frac{R_2}{R_1 + R_2} \qquad \ldots (17.12)$$

and the sampled voltage fed back is

$$V_f = \beta V_L \qquad \ldots (17.13)$$

This voltage is compared with the reference voltage V_Z provided by a Zener. This reference voltage is applied to the non-inverting input of the op amp the difference between V_Z and V_f is known as error voltage. It is amplified by the op amp error amplifier, which controls the base current of the series pass transistor Q. If for any reason the load (output) voltage decreases, V_f decreases accordingly and the base current of the transistor increases significantly. This leads to a decrease in the internal resistance of the transistor consequently decreasing the voltage drop across it. Thus increasing the voltage across the load. If the load voltage increases for any reason. V_f increases leading to

consequential increase in the voltage drop across it. Thus decreasing the voltage drop across the load. The series element (also called pass transistor) transistor thus behaves as a variable voltage controlled resistor and provides stabilization of the output voltage against changes in V_i and I_L.

17.6 VERSATILE VARIABLE VOLTAGE IC REGULATOR (IC 723)

The electronic voltage regulator described in the previous section can be fabricated on a single chip thus offering, low cost, high performance, small size and easy to use. The basic circuit of voltage IC 723 regulator is shown in figure 17.4. This circuits consists of voltage reference source, an error amplifier, a series pass transistor, and a current limiting transistor and the positive voltage regulator circuit is shown in Fig. 17.5.

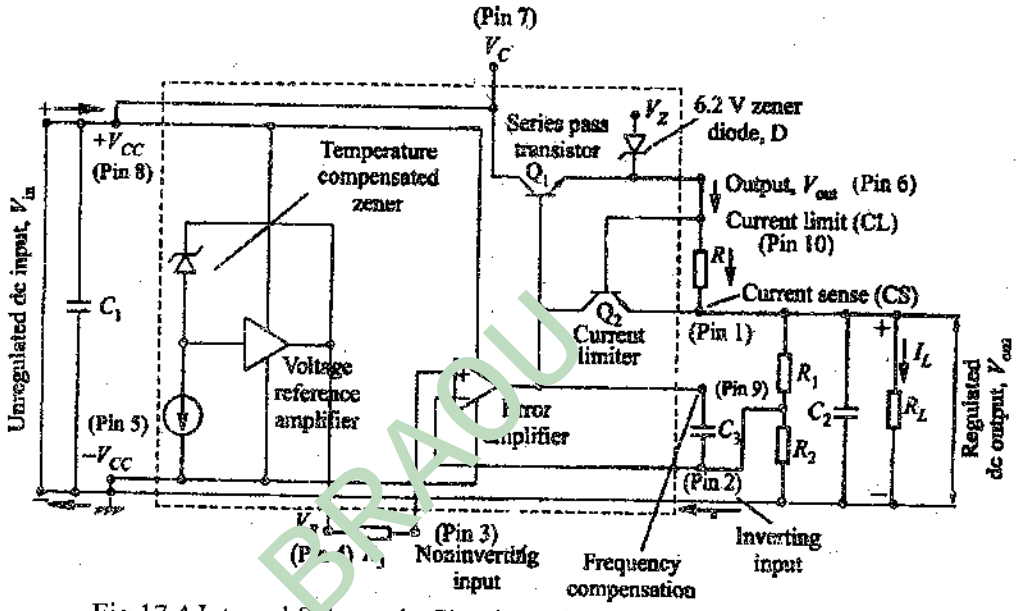

Fig 17.4 Internal Schematic Circuitry of the LM723 IC Voltage Regulator (positive voltage Regulator)

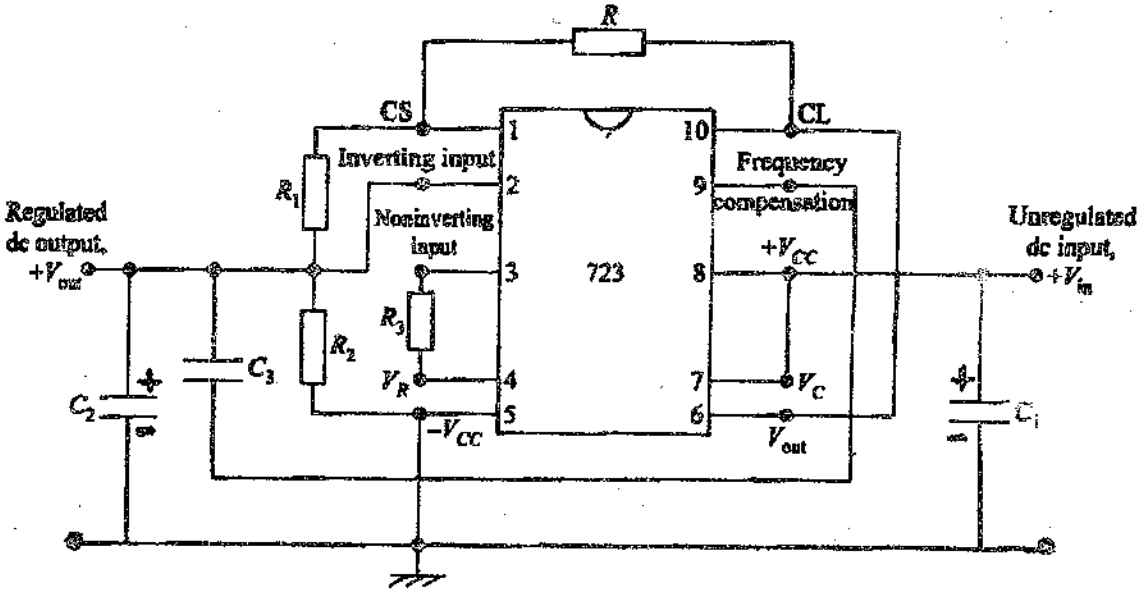

Fig 17.5 The Circuit Diagram of Positive Voltage Regulator using 723 IC

difference between these two voltages whenever any fluctuation in output voltage arises. The transistor Q_1 is also connected as an emitter follower and a fraction of the output is sampled by the potential divider network R_1 and R_2 and fed back to the inventing terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage connecting to the non inverting terminal of the amplifier . The output V_0' of the error amplifier drives the series transistor Q_1.

If the output voltage increase, due to variation in load current, the sampled voltage βV_0 also Increases, where $\beta = \frac{R_2}{R_1 + R_2}$. This reduces the output voltage V_0' of the amplifier due to the 180^0 out of phase provided by the op-amp amplifier. So, the input to the base of Q_1 decreases. hence, that is V_0 also reduces. Hence the increase in V_0 is nullified.
Similarly reduction in output voltage also gets reduced.

Let us consider the 1C723 general-purpose regulator shown in figure 12.33. It can be easily adjusted for a wide range of positive or negative voltage. This IC is inherently low current device, but can be boosted to provide more current by connecting external components. The limitation of 723 is, it has no in built thermal protection. It also has no short circuit current limits.

The functional block diagram of IC723 regulator is shown in figure 12.29. It has two separate sections.

(i) The Zener diode, a constant current source and reference amplifier section, it produces a fixed voltage. The constant current source forces the Zener to operate at a fixed point so that zener diode outputs a fixed voltage.

(ii) The other section of a IC consists of an error amplifier, a series pass transistor Q_1 and current limiting transistor Q_2. The error amplifier compares a sample of the output voltage fed from section I applied to the negative terminal (inverting terminal) and the reference voltage applied to the positive terminal (non inverting terminal). If there is any error, then error signal controls the conduction of Q_1.

The output voltage V_0 is given by

$$V_O = V_{ref} \frac{R_2}{R_1 + R_2}$$

If the output voltage becomes low, the voltage at the inverting terminal of error amplifier also goes down. This makes, the output of the error amplifies to become more resistive, thereby driving transistor Q_1 more into conduction. This reduces the voltage across Q_1 and drives more current into the load causing the voltage across load to increase. So the initial drop in the load voltage has been compensated. Similarly any increase in load voltage, or changes in the input voltage get reduced.

17.7 FIXED VOLTAGE IC REGULATOR

IC 723 is a sophisticated versatile regulator, which requires some designing. However, for several applications only certain fixed voltage are required. For such applications specialized fixed voltage 3-pin regulator IC's are developed. It is very simple to use.

They have a only 3-terminals. The unregulated input voltage is applied to the input terminal. The regulator output is taken from the output terminal. The references or adjust terminal is normally grounded or in some cases maintained at certain reference voltage

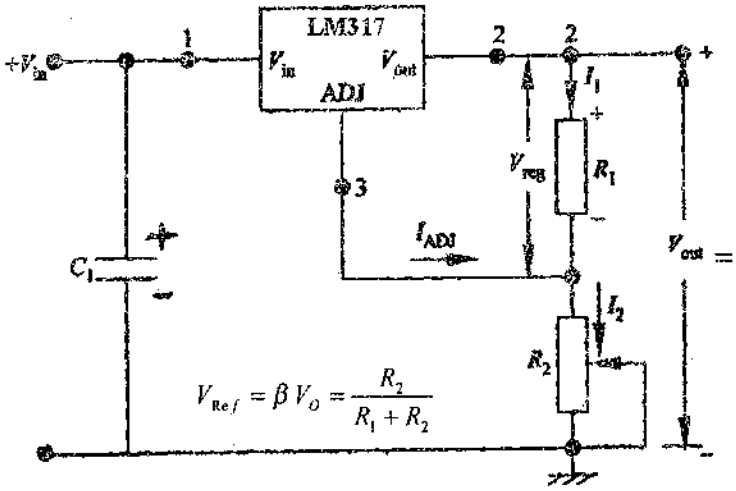

Fig 17.6(a) Fixed +ve Voltage Regulator

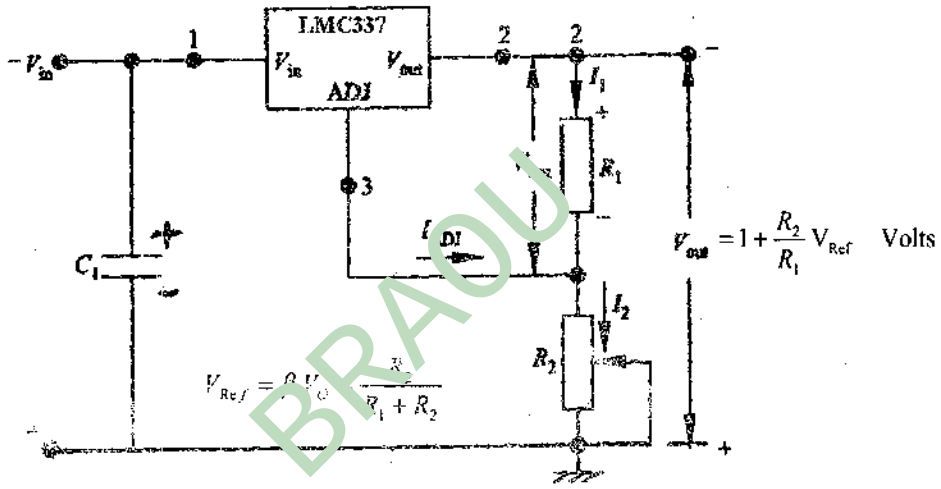

Fig 17.6(b) fixed -ve Voltage Regulator

V_{Ref} derived from the regulator output as shown in Fig 17.6.(a,b). There are both positive voltage regulators and negative voltage regulators. The voltage retains vary from 5V, 6V, 9V 12V, 15V..... 45V and the current rating vary between 150 mA to 1 Amp.

The positive voltage regulators are LM317, LM320, ...,78XX etc. where XX standards for the voltage range like 05, 08, 12, 15 etc. Similarly negative voltage regulators are LM337, LM330 .....79XX , etc. where again XX stands for the voltage range. The circuit diagram of positive voltage regulator and a negative voltage regulator are shown in Fig.

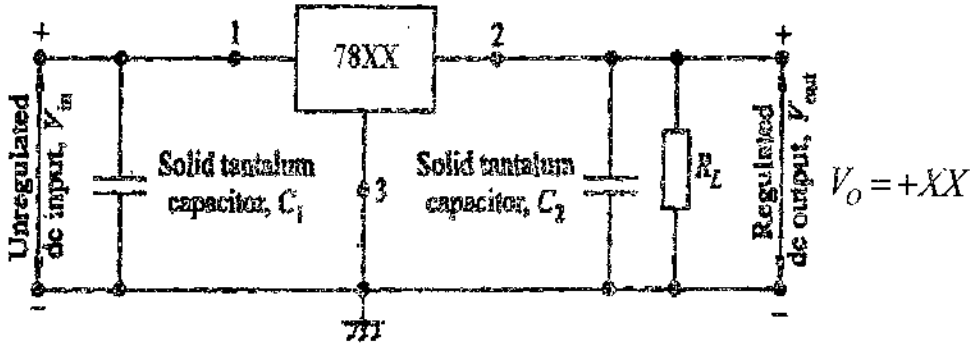

Fig 17.7(a) Fixed 3-pin +Ve Voltage Regulator

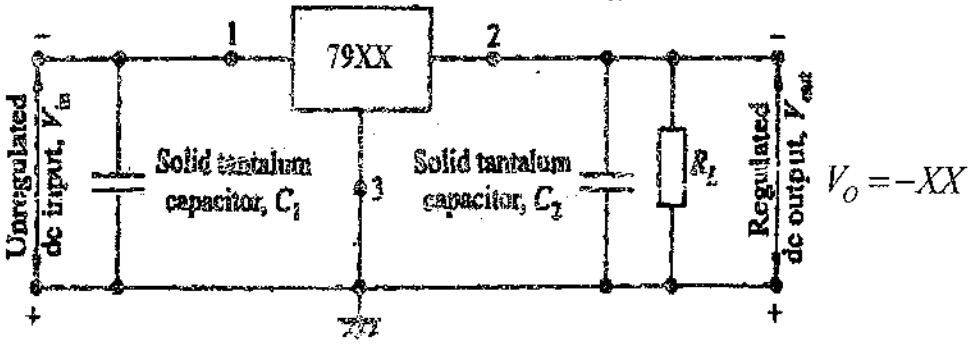

Fig 17.7(b) Fixed 3-pin -Ve Voltage Regulator

17.8 SWITCH MODE REGULATOR POWER SUPPLY (SMPS)

17.8.1 Comparative Study of SMPS and Linear Power Supplies

So far we have discussed some linear mode power supplies. They suffer from the following limitations.

(i) The input step-down transformer is bulky and it is the most expensive component because its operating frequency is very low (say 50Hz). Because of this low frequency large value of filter capacitor is required to decrease the ripple.

(ii)The efficiency is very low because the difference between the input voltage and output voltage is very high. This results in large power dissipation across series pass transistor.

(iii) The linear mode power supply requires additional ± 15 V dc source to operate the active device such as op-amp, it may not be economically and practically feasible.
(iv) For a specified range of input-output variation linear regulator maintain constant output voltage by dissipating the excess power as heat. Due to this reasons, the linear regulators is suited for medium current applications only.

In order to overcome the above limitations, switch mode power supplies SMPS are used. The block diagrammatic representation of switching regulator is shown in figure 17.8.

In a linear mode power supply the series pass transistor is operated in the active region, but in a switching regulator, the series pass transistor is switched between cutoff and saturation levels at a high frequency which produces a pulse width modulated (PWM) square wave output. This output is filtered through a low pass LC filter to produce an average dc output voltage.

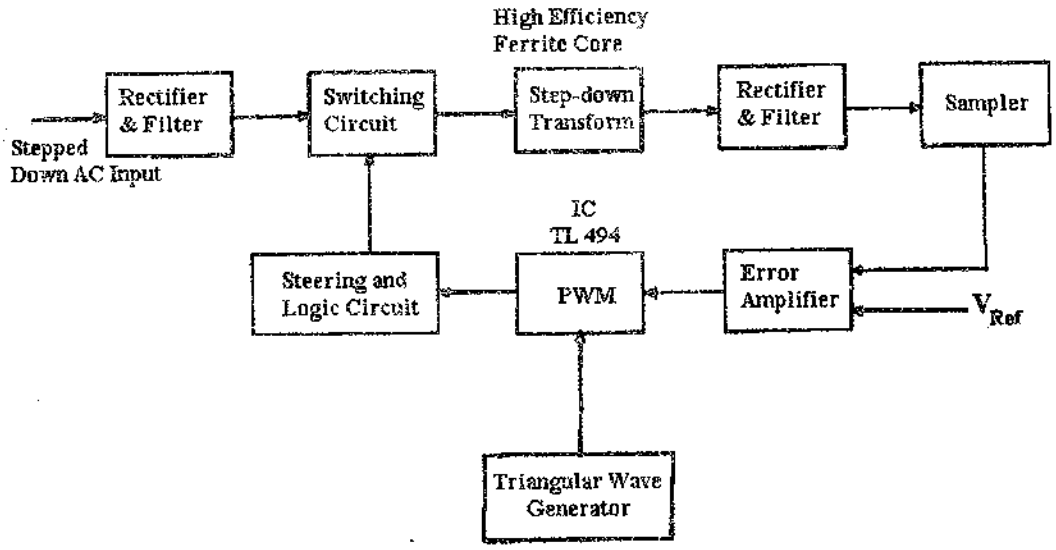

Fig 17.8 Block Diagram of SMPS

Thus the output voltage is proportional to the pulse width and switching frequency. The efficiency of switching regulator is independent of the input-output voltage thus it approach 95%.

17.8.2 Disadvantages of Linear regulators

- Since the line frequency is SO Hz the step down transformer, which is the first functional block, is bulky and costly.
- Large values of capacitors are required to reduce the ripple.
- Vin should be greater than Vo since there is always a drop across the series element, which is always in the active region.
- Due to this the power dissipated across the active device is more and hence power transmitted to the load is less which reduces the efficiency to 25 - 50 %

17.8.3Advantages of SMPS

- Does not require a step-down transformer at the input.
- Since the pass transistor is operated as a switch the power dissipated across it is negligible and hence power transmitted to the load is maximum and this improves the efficiency to 70 -90 %.

17.9 CIRCUIT DESCRIPTION OF SMPS

The circuit diagram of simple SMPS is shown in Fig 17.9

1.The rectifier circuit is used to convert the ac input into a pulsating DC, which in turn is purified using filter networks.

2.The Switching circuit consists of two transistors Qi and Q2 that are driven by the output of the steering and logic circuit. If the output of the logic circuit is high, the transistor is taken to saturation and if the output is low, the transistor is taken to cut-off. Thus the transistors are either ON or OFF based on the output of the logic circuit.

3.The alternating outputs of the switching circuit is stepped down in voltage by the

transformer and fed to the rectifier and filter sections to obtain a pure dc.

4.The block 4 is a sampler network, which is a simple voltage divider network that takes part of the output and feeds it to an error amplifier.

5.The error amplifier compares this with a reference voltage and amplifies the difference.

6.The output of the error amplifier is fed to a pulse width modulator (PWM) circuit. PWM is a circuit, which gives an output pulse whose width is a function of voltage. An op-amp Comparator performs this function. Comparator is a circuit, which operates the op-amp in the open loop where the gain is infinity and the output swings between positive saturation and negative saturation based on whether the difference is positive or negative.

7.The PWM circuit takes a DC voltage and a triangular wave as inputs. If the DC voltage is less than the triangular wave input, the output of the Comparator is high and if the dc voltage is more than the triangular wave input, the output of the Comparator is low.

8.The logic circuit consists of 2 logic AND gates. One input of both the AND gates is obtained from the output of the pulse width modulator. The other input of AND gate 1 is got from the output Q of the Flip-flop while the other input of AND gate 2 is got from the output $\overline{Q}$ of the Flip-flop.

17.10 THEORY OF SWITCHING REGULATORS

It produces an symmetrical square wave varying in either frequency or pulse width called frequency or pulse width modulation. The frequency range of pulse generator for optimum efficiency is 20 KHz

The duty cycle of the pulse waveform determines the relationship between the input and output voltages. The duty cycle is the ratio of the ON time to period 'T' of pulse waveform i.e.,

$$DutyCycle = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{t_{ON}}{T} = t_{ON} \bullet f \qquad \ldots(17.14)$$

where t_{ON} = on time of the pulse waveform

t_{OFF} = off time of the pulse waveform

$$T = \text{time period} = t_{ON} + t_{OFF} = \frac{1}{f}$$

There are some trades off between the operating frequency and efficiency High operating frequency reduce the ripple voltage at the expense of decreased efficiency and increase the noise. On the other hand lower operating frequency improve the efficiency and reduce the noise but ripple are high hence it require large filter components.

4. Filter

Filter converts the pulse from the output of the switch into a dc voltage. The RLC filter is must commonly used in the switching regulator.
The output voltage of switching regulator is a function of duty cycle and the input voltage yin.

i.e., $$V_O = \frac{t_{ON}}{t + t} \bullet V_{in} = \frac{V_{in} t_{ON}}{T} \qquad \ldots(17.15)$$

In the above equation____ , if the time period 'T' is constant, V_0 is directly proportional to the ON-time 't_{ON}' for a given value of V_{in}. This method of changing output voltage by varying t_{ON} is referred to as "pulse width modulation".

Similarly if t_{ON} is held constant, the output voltage is inversely proportional to the period "T" or directly proportional to $\left(i.e., f = \frac{1}{T}\right)$ frequency 'f' of pulse waveform, then it is known as "frequency modulation".

Circuit operation

On switching on the mains, the first functional block coverts the ac into a pure form of DC and is obtained at the output. Part of the output is taken through the sampler network and is fed to the error amplifier, which gives a DC voltage as output on comparing with a reference voltage. If V_0 is high, the output of the error amplifier V~. is high and this is compared with the triangular waveform. When V~ is greater than the triangular input, the output of the PWM is low and if V~ is lower than the triangular input, the output of PWM is high. Thus the value of V~ decides how long the output of the PWM is high or in other words the pulse width. Hence the pulse width is less for a high V~ and vice-versa. The output of the PWM is used to drive the logic gates A and A,. The other input to the gate comes from the Flip-Flop circuit. The flip-flop circuit gives an output as high or low alternatively for every clock pulse. When its output Q is high, Q' is low and vice-versa. ~ gets the input from Q and output of PWM while A, gets the input from Q' and output of PWM and so only one of the gates give a logic high at a time. Based on the output of the PWM, the output of the gates remains high to drive the transistor Q_1 or Q_2. If V_0 goes high due to variations in line voltage or load variations, V~ becomes high, which reduces the pulse width. Therefore, the output of the gate is high for a short duration and hence the transistor remains ON for a small duration, which reduces the output and brings it down to the original value.

17.12 COMPARISION OF LINEAR POWER SUPPLY AND SMPS

Parameter	Linear Power Supply	SMPS
Size	Large	Small
Weight	Heavy	Light
Efficiency	Poor (25 – 50%)	Good (65-80%)
Operating Task	High	Low
Noise Level at Output	Low	High
Mains Transformer	Bulky	Small
Filter Capacitor	Bulky	Medium
Transformer Core	Laminated Iron	Ferrite Core
Regulation	Less than 0.1%	0.3%
RF interference	Special shielding should be provided	Negligible

17.12.1 Buck - Boost Cuk Switched Mode Regulator:

This circuit operates on the principle of both Buck (Step Down) and Boost (Step Up) converter. It's a simplified and cascaded converter utilizing minimum number of switched

the input voltage but with in opposite polarity to that of the input voltage.

When transistor switch tube is OFF, the capacitor C_1 charges through the inductor L_1 and the diode D. When the transistor switch turned ON, the discharging current of the capacitor C_1 consists of two parts namely one part charges the capacitor C_2 through C_1 inductor L_2, and transistor Q. The second part flows through the load R_L and inductor L_2, capacitor C_1 and transistor Q.

When the Transistor is OFF, the stored energy in the inductor L_2 reverses its polarity and sends and drives current into the load R_L through the diode D, while the voltage is maintained by capacitor C_2. All the energy stored in a inductor L_2 is used up, capacitor C_2 discharges and the output voltage decreases. This regulator can be used both as step up or step down transformer with reversed polarity.

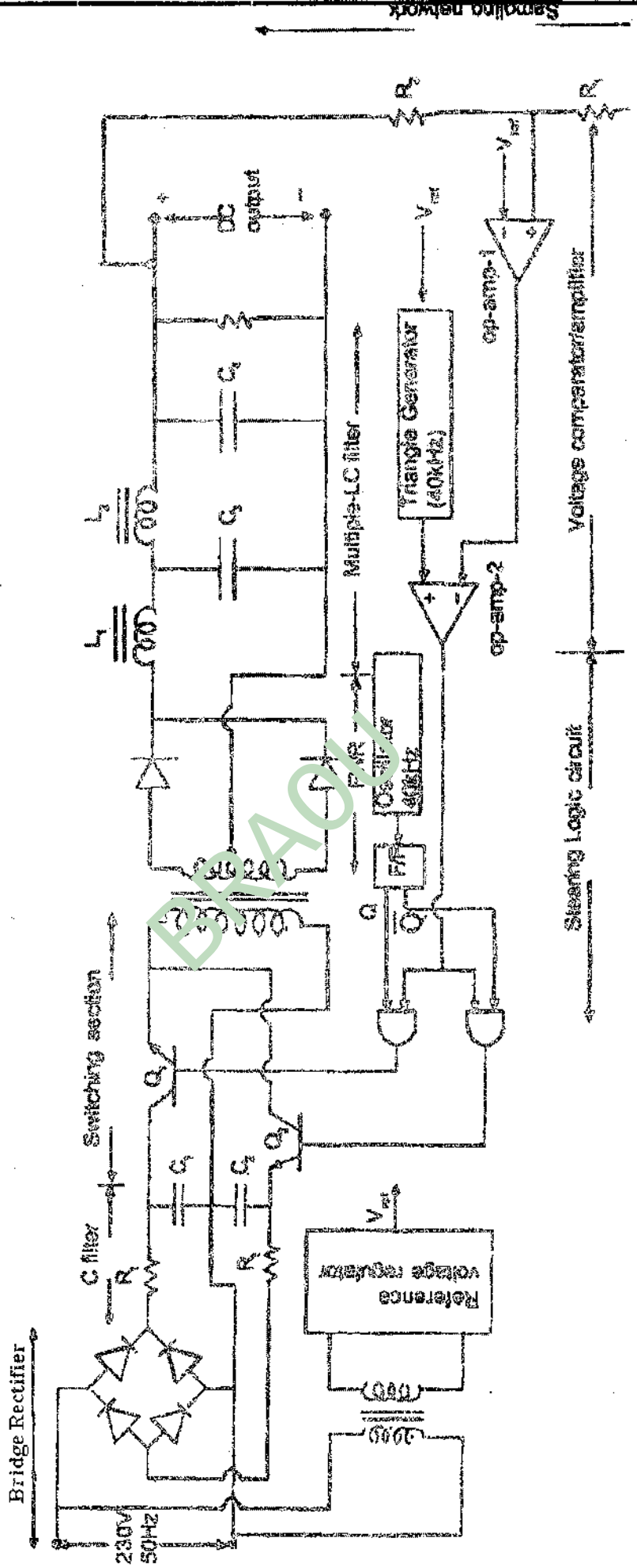

Fig 17.9 Circuit Diagram of SMPS

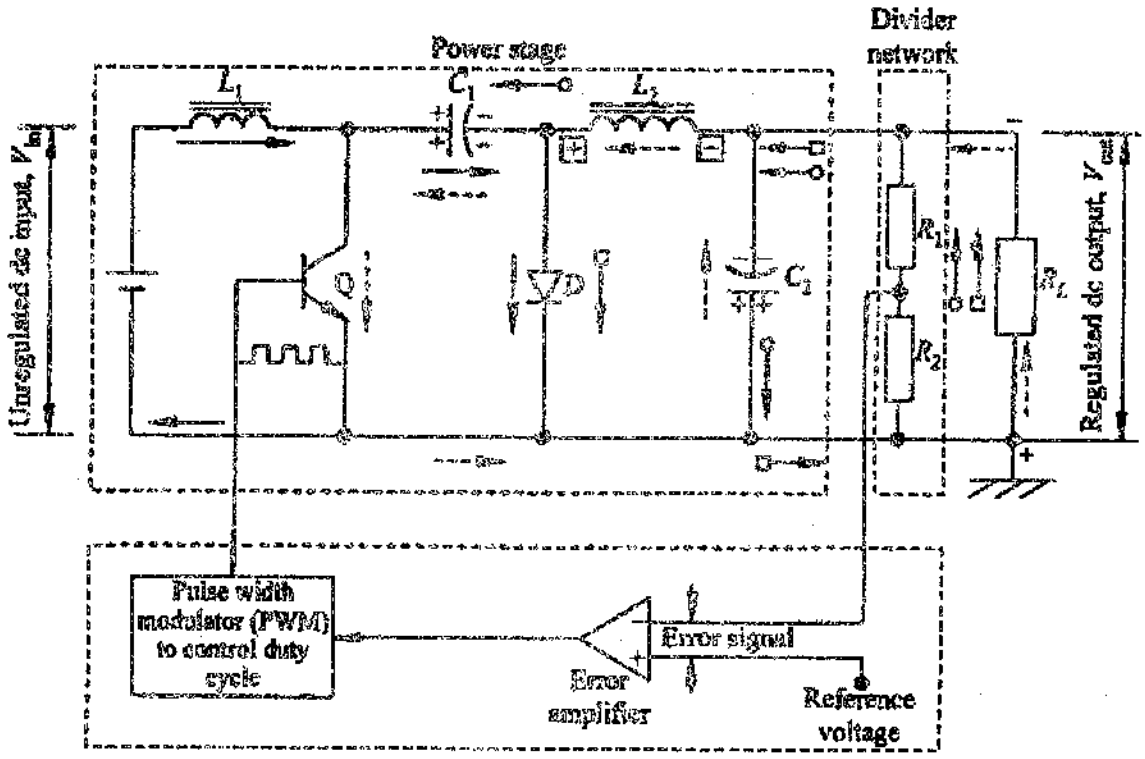

Fig 17.10 Circuit Diagram of Buck Boost Converter

17.12 SUMMARY

Zener regulator and electronic regulator give a constant voltage output

$$\% \text{ regulation} = \frac{V_{OC} - V_L}{V_L R_L} X100$$

Where V_{OL} is the output voltage under no load condition V_L output voltage under load R_L load resistance

17.13 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the circuit diagram of a simple Zener voltage regulator and explain its regulator action
2. Draw the circuit diagram of an electronically regulated power supply and explain its working.
3. Which of the following Viz the Zener or the series type of regulator is a better regulator? What are the other reasons for opting for series electronic regulation than shunt regulator?

1. Define voltage regulation and explain its need.
2. Discuss the action of the Zener regulator.

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17.15 GLOSSARY

Rectifier	:	A system of diodes that convert ac voltage into unidirectional but Pulsating voltage
Filters	:	Frequency selective circuits that smoothen the pulsating voltages.
Voltage multiplied	:	A process in which the given voltage is by Multiplication an integral number.
Ripple current.	:	The ac component of a rectified voltage or
Voltage Regulators	:	Electronic circuits, which maintain a rated, output voltage under all conditions either no load or full load.

BLOCK – VI

MEASURING INSTRUMENTS

UNIT–18 ANALOG MEASURING INSTRUMENTS

Contents:

18.0 AIMS AND OBJECTIVES

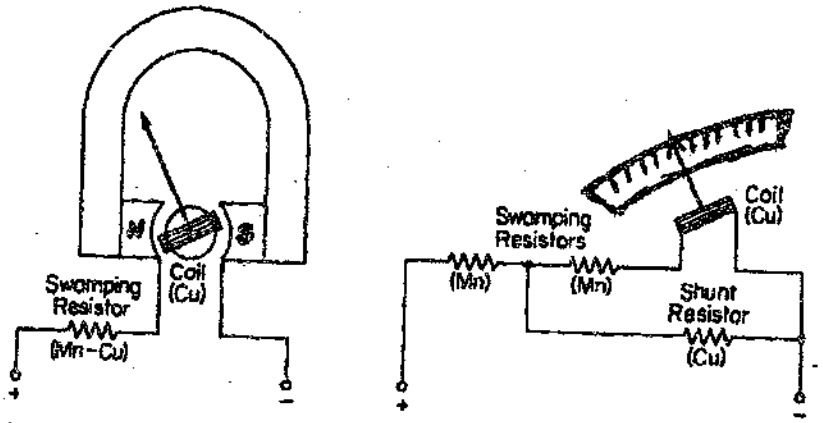
This unit introduces you to the concepts of designing of passive. DC ammeters, DC voltmeter, ohmmeters, AC voltmeter. This unit also introduces you to the design of FET input type Electronic voltmeters.

18.1 INTRODUCTION

The constructional details of PMMC type of OC micro ammeters is the basic for almost all the passive measuring instruments like the Voltmeter, Ammeter, Ohmmeter. This improvement in accuracy measurement. As achieved by the use of FET input type of measuring instruments.

18.2 d'ARSONVAL TYPE MEASURING INSTRUMENT

The constructional details of a d'Arsonval type of suspension galvanometer is shown in Fig18.1. It is designed on the principle of a permanent magnet moving coil (PMMC) type of suspension galvanometer. A coil is suspended in the magnetic field of a horseshoe type of a permanent magnet, so that it can rotate freely in the magnetic field. When current flows in the coil, the magnetic field developed in the coil interacts with the permanent magnetic field and developed electromagnetic (EM) torque causes the coil to rotate. The EM torque is counterbalanced by the mechanical torque of control springs attached to the movable coil.



(a) Simple compensation circuit.

(b) Improved compensation using series and shunt resistors.

Fig. 18.1 The d' Arsonval PMMC type of meter

The balance of torques, and therefore the angular position of the movable coil, is indicated by a pointer against a fixed reference, scale attached to the mechanism. The equation for the developed torque, derived from the basic law for electromagnetic torque, is

$$T = B \times A \times I \times N \qquad \ldots(18.1)$$

The restoring mechanical torque due to the suspension springs try to counter balance the rotation of the coil, and is given by

$$T = C \times \theta \qquad \ldots(18.2)$$

where T = torque [newton-meter (N-m)]

B = flux density in the air gap [webers/square meter (tesla)]
A = effective coil area [square meters (m^2)]
I = current in the movable coil [amperes (A)]
N = turns of wire on the coil
C= Restoring couple for unit rotation exerted by mechanical suspension Springs
θ = The angular defelction

$$\text{Hence, } B \times A \times I \times N = T = C \times \theta \qquad \ldots (18.3)$$

$$\text{Or} \quad I \propto \theta \qquad \ldots (18.4)$$

The current flowing through the coil is proportional to the deflection of the coil

18.3 CONVERSION OF D'ARSONVAL PMMC TYPE OF DC MICRO AMMETER IN TO AN AMPERE METER OF HIGHER RANGES

The basic movement of a dc ammeter is a PMMC type galvanometer. The coil can carry only very small currents of few tens of microamperes. When large currents are to be measured, it is necessary to bypass the major part of the current through a shunt resistance, as shown in Fig.18.2. The resistance of the shunt can be calculated by applying conventional circuit analysis, where

R_m = internal resistance of the movement (the coil)
R_S = resistance of the shunt
Im = full-scale deflection current of the movement
I_S = shunt current
I = Total Input current to be measured by the ammeter including the shunt resistance

Since the shunt resistance is in parallel with the meter movement, the voltage drops across the shunt and movement must be the same and hence we can write

$$V_{shunt} = V_{movement} \qquad \ldots(18.5)$$

or

$$I_S R_S = I_m R_m \quad \text{and} \quad R_S = \left(\frac{I_m R_m}{I_S} \right) \qquad \ldots (18.6)$$

Since $I = I_S + I_m$, we can write or $I_S = I - I_m$ ...(18.7)

$$R_S = \left(\frac{I_m R_m}{I - I_S} \right) \qquad \ldots (18.8)$$

For each value of full-scale current to be measured, the value of the shunt resistance required is calculated with the help of relation 18.8.

EXAMPLE 18-1

A 1-mA meter movement with an internal resistance of 100Ω is to be converted into a 0-100-mA ammeter. Calculate the value of the shunt resistance required.

SOLUTION

$I_S = I - I_m = 100\text{-}1 = 99$ mA

$$R_S = \frac{I_m R_m}{I_S} = \frac{1mA X 100\Omega}{99mA} = 1.01\Omega$$

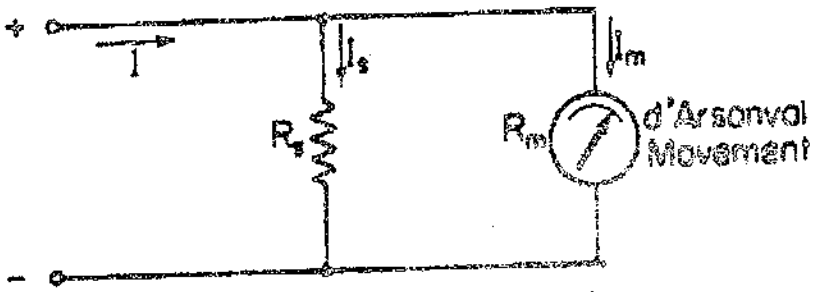


Figure 18.2 Basic dc ammeter circuit.

18.4 AYRTON SHUNT AND MULTI RANGE AMMETER

The current range of the dc ammeter may be further extended by providing a large number of shunts selected by a range switch. Fig.18.3(a) shows the schematic diagram of a multi range ammeter. Four shunts, R_a, R_b, R_c, and R_d, which can be placed in parallel with the movement to give four different current ranges. Switch S is a multi position, make or break type switch. The problem associated with this type of circuit is that the dc meter is not protected while different current ranges re selected. Hence, a

modified circuit shown in Fig. 18.3(b) is adopted

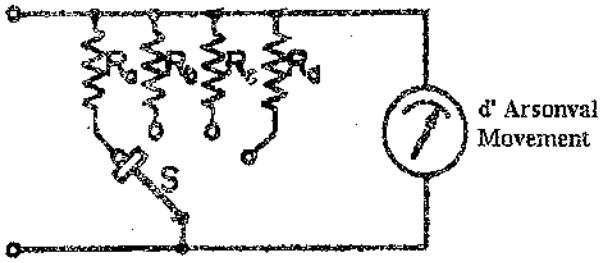


Figure 18.3(a) Schematic diagram of a simple multirange ammeter.

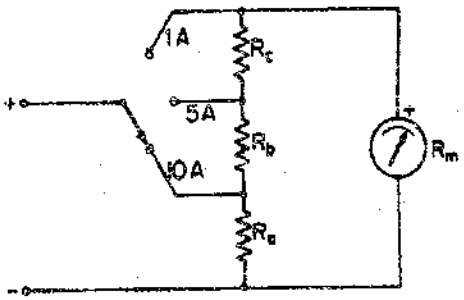


Figure 18.3(b) Universal or Ayrton shunt.

This universal, or Ayrton, shunt of Fig. 18.3(b) eliminates the possibility of having the meter in the circuit without a shunt. This advantage is gained at the price of a slightly higher overall meter resistance. Since at any achieved position of the switch any one of the shunt resistances. This calculation indicates that for larger currents the value of the shunt resistor may become very small.

Direct-current ammeters are commercially available in a large number of ranges from 20 μ A to 50 A full-scale for a self-contained meter and to 500 A for a meter with external shunt.

The following precautions should be observed when using an a ammeter in measurement work:

(a) Always connect an ammeter in series with a load capable of limiting the current. But never connect an ammeter across (in parallel with) a source of emf. Because of its low resistance it would draw damagingly high currents and destroy the delicate movement.

(b) Observe the correct polarity while connecting the meter. Reverse polarity causes the meter to deflect against the mechanical stop and this may damage the pointer.

(c) When using a multirange meter, first use the highest current range; then decrease the current range until substantial deflection is obtained.

18.5 CONVERSION OF A D'ARSONVAL PMMC TYPE MICRO AMMETER IN TO VOLTMETER

The addition of a series resistor, or multiplier, converts the basic d'Arsonval movement into a dc voltmeter, as shown in Fig. 18.4 which limits the current through the movement so as not to exceed the value of the full-scale deflection current (I_{fs}). A dc voltmeter measures the potential difference between two points in a dc circuit and is therefore connected across a source of emf or a circuit component. The meter terminals are generally marked "+" and "--," since polarity must be observed strictly as shown in case of measurement.

The value of a multiplier series resistance, required to convert a micro ammeter into voltmeter is calculated as follows, referring to Fig.18.4

$$V = I_m (R_S + R_m)$$

$$\text{Or } I_m R_S = V - I_m R_m \qquad \ldots(18.9)$$

$$R_S = \frac{V - I_m R_m}{I_m} = \frac{V}{I_m} - R_m \qquad \ldots(18.10)$$

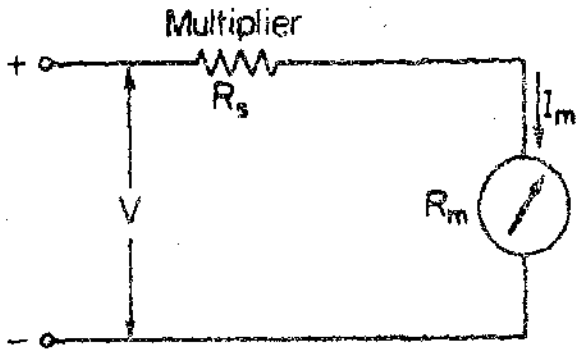


Figure 18.4 Basic DC voltmeter circuit

where

I_m=deflection current of the movement (I_{fsd})

R_m= internal resistance of the movement

R_S =multiplier resistance

V = full-range voltage of the instrument.

The multiplier resistors are usually mounted inside the case of the voltmeter for moderate ranges up to 500 V. For higher voltages, the multiplier ma be mounted separately outside the case on a pair of binding posts to avoid excessive heating inside the case.

18.6 CONVERSION OF A MICRO AMMETER INTO MULTI RANGE VOLTMETER

The addition of a large number of multiplier resistors, together with a range switch, provides the instrument with a workable number of voltage ranges. Figure 18.5(a) shows a multirange voltmeter using a four-position switch and four multipliers, R_1, R_2, R_3, and R_4, for the voltage ranges V_1, V_2, V_3, and V_4 respectively. The values of the multipliers can be calculated using the relation 18.10.

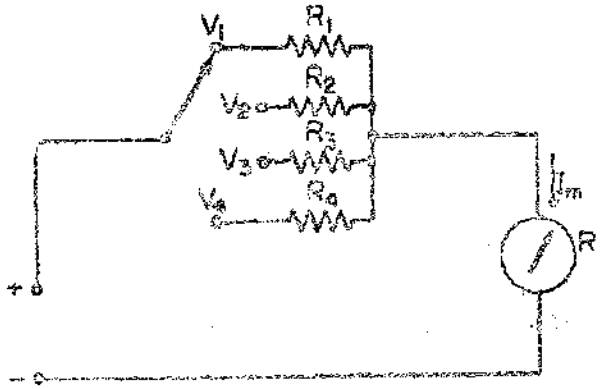


Figure 18.5(a) multi range Voltmeter

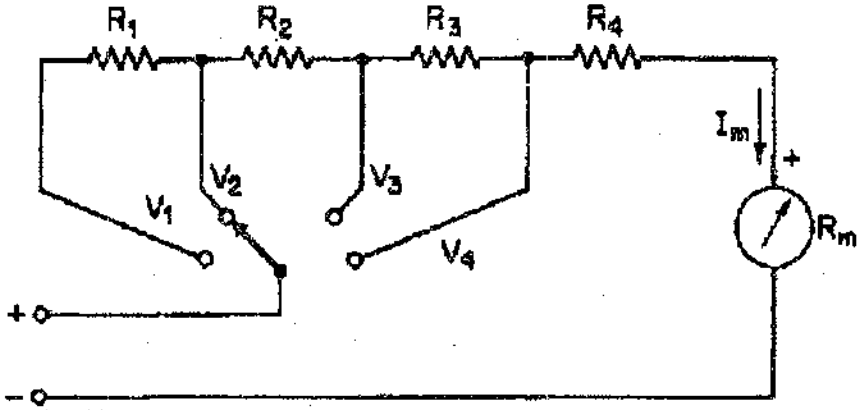


Figure 18.5(b) More practical arrangement of multiplier resistors in the multi range voltmeter.

A variation of the circuit of Fig. 18.5(a) is shown in Fig. 18.5(b), where the multipliers are connected in a series string and the range selector switches the appropriate amount of resistance in series with the movement. This system has the advantage that all multipliers except the first are standard resistances and can be obtained commercially in precision tolerances. The low-range multiplier, R_4, is the only special resistor that must be manufactured to meet the specific circuit requirements.

18.7 CONVERSION OF MICRO AMMETER INTO A SERIES-TYPE OHMMETER

The series-type ohmmeter shown in fig 18.6 essentially consists of a d'Arsonval movement connected in series with a resistance and a battery to a pair of terminals to which the unknown resistance R_X is connected. The current through the movement then depends on the magnitude of the unknown resistor, and the meter indication is proportional to the value of the unknown resistance. When the unknown resistor $R_X = 0$ (terminals A and B shorted), maximum current flows in the circuit. Under this condition, shunt resistor R_2 is adjusted until the movement indicates full-scale current (I_{fsd}). The full-scale current position of the pointer is marked "0Ω" on the scale. Similarly, when $R_X = \infty$ (terminals A and B open), the current in the circuit drops to zero and the movement indicates zero current, which is then marked "∞" on the scale. Intermediate markings may be placed on the scale by connecting different known values of R_X to the instrument. Although the series-type ohmmeter is a popular design and is used extensively in portable instruments for general-service work, it has certain disadvantages. Important among these is the internal battery whose voltage decreases gradually with time, so that the full-scale current drops and the meter does not read "0" when A and B are shorted. The variable shunt resistor R_2 in Fig.19.6 provides an adjustment to counteract the effect of decease in battery voltage. Without R_2, it would be possible to bring the pointer back to full scale by adjusting R_1, but this would change the calibration all along the scale.

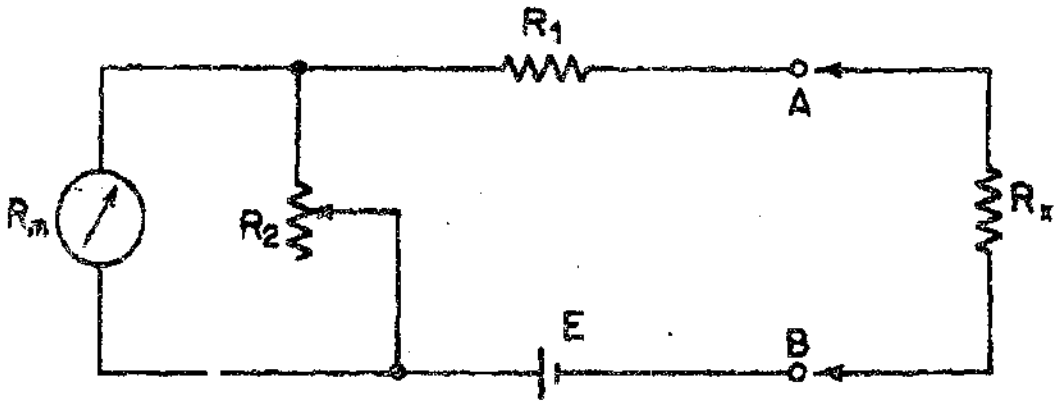


Figure 18.6 Series Type Ohmmeter

Where

R_1=current-limiting resistor

R_2= zero adjust resistor

E = internal battery

R_m = internal resistance of the d'Arsonval movement

R_X= unknown resistor

Adjustment by R_2 is a superior solution, since the parallel resistance of R_2 and the coil R_m is always low compared to R_1 and therefore the change in R_2 needed for adjustment does not change the calibration very much.

A convenient quantity to use in the design of a series-type ohmmeter is the value of R_X, which causes half-scale deflection of the meter. At this position, the resistance across terminals A and B is defined as the half-scale position resistance given the full-scale current I_{fsd} and the internal resistance of the movement R_m battery voltage E, and the desired value of the half-scale resistance R_h, the can be analyzed as shown below

$$R_h = R_1 + R_2 \parallel R_m$$

or

$$R_h = R_1 + \frac{R_2 R_m}{R_2 + R_m} \qquad \ldots(18.11)$$

The total resistance presented to the battery then equals $2R_h$, and the battery it needed to supply the half-scale defection is

$$I_h = \frac{E}{2R_h} \qquad \ldots(18.12)$$

To produce full-scale deflection, the battery current must be doubled, and there

$$I_t = 2I_h = \frac{E}{R_h} \qquad \ldots(18.13)$$

The shunt current through R_2 is

$$I_2 = I_t - I_{fsd} \qquad \ldots(18.14)$$

The voltage across the shunt (E_{Sh}) is equal to the voltage across the movement and

$$E_{Sh} = E_m \text{ or } I_2 R_2 = I_{fsd} R_m$$

$$R_2 = \frac{I_{fsd} R_m}{I_2} \qquad \ldots(1815)$$

Substituting Equ. (18.14) Into Equ. (18.15), we obtain

$$R_2 = \frac{I_{fsd} R_m}{I_t - I_{fsd}} = \frac{I_{fsd} R_m R_h}{E - I_{fsd} R_h} \qquad \ldots(18.16)$$

Solving Equ. (18.11) for R_1 gives

$$R_1 = R_h - \frac{R_2 R_m}{R_2 + R_m} \qquad \ldots(18.17)$$

Substituting Equ. (18.16) into Equ. (18.17) and solving for R yields

$$R_1 = R_h - \frac{I_{fsd} R_m R_h}{E} \qquad \ldots(18.18)$$

18.8 RECTIFIER TYPE ALTERNATING CURRENT INDICATING INSTRUMENTS

The d'Arsonval movement responds only to the average or dc value of the current through the moving coil. If the movement carries an alternating current with positive and negative half-cycles, the driving torque would be in one direction during the positive half cycle and in the other direction during the negative half cycle. If the frequency of the ac is very low, the pointer would swing back and forth around the zero point on the meter scale. At higher frequencies, the inertia of the coil is so great that the pointer cannot follow the rapid reversals of the driving torque and hovers around the zero mark, vibrating slightly.

The rms and x values of the current are shown by the relations (18.19) and (18.20)

$$I_{rms} = \frac{2I_{max}}{\sqrt{2}} = \frac{I_{max}}{\sqrt{2}} = 0.707 I_{max} \qquad \ldots(18.19)$$

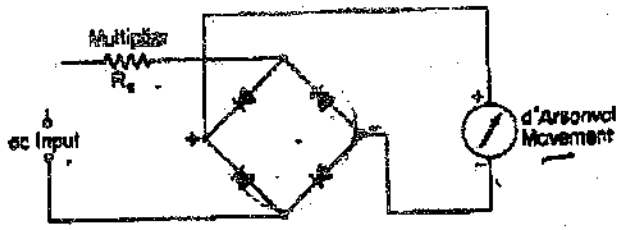
$$I_{DC} = \frac{2}{\pi} I_{max} = 0.636 I_{max} \qquad \ldots(18.20)$$

To measure ac on a d'Arsonval movement, some means must be devised to obtain a unidirectional torque that does not reverse during each half-cycle. One method involves rectification of the AC, so that the rectified current always flows in the coil in one direction and deflects the coil also in one direction.

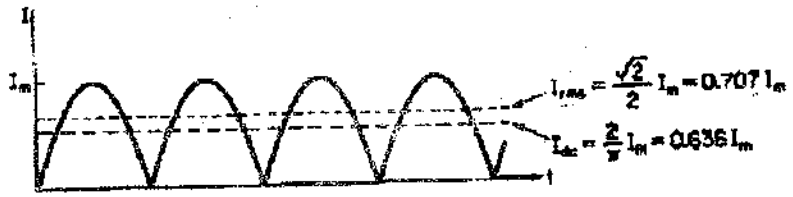
Other methods use the heating effect of the alternating current to produce an indication of its magnitude. However, theyare beyond the scope of this chapter.

One obvious answer to the question of ac measurement is found by using a rectifier to convert ac into a dc and then to use a dc movement to indicate the value of the rectified ac.

Rectifier-type instruments generally use a PMMC movement in combination with a rectifier arrangement as shown in fig 18.7.



(a) Circuit



(b) Rectified Current Through Meter Movement

Fig. 18.7 Full Wave Rectifier

movement over the complete cycle of the input voltage. Because of the inertia of the moving coil, the meter will indicate a steady deflection proportional to the average value of the current. Since alternating currents and voltages are usually expressed in rms values, the meter scale is calibrated in terms of the rms value of a sinusoidal waveform.

18.9 FET INPUT TYPE ELECTRONIC VOLTMETER

A simple amplifier type of electronic voltmeter is shown in Fig. 18.8. This meter greatly reduces the amount of power drawn from a circuit under test by increasing the input impedance using an amplifier with unity gain. A source follower drives an emitter follower. This combination is capable of achieving thousand-fold increase input impedance, while maintaining a voltage gain of very nearly one. The input impedance of this meter is 10 MΩ, which would require 0.025 μ W of power for a 0.5-V deflection, as compared to 25 μ W for for passive meter. An increase sensitivity of hundred times is achieved through this arrangement.

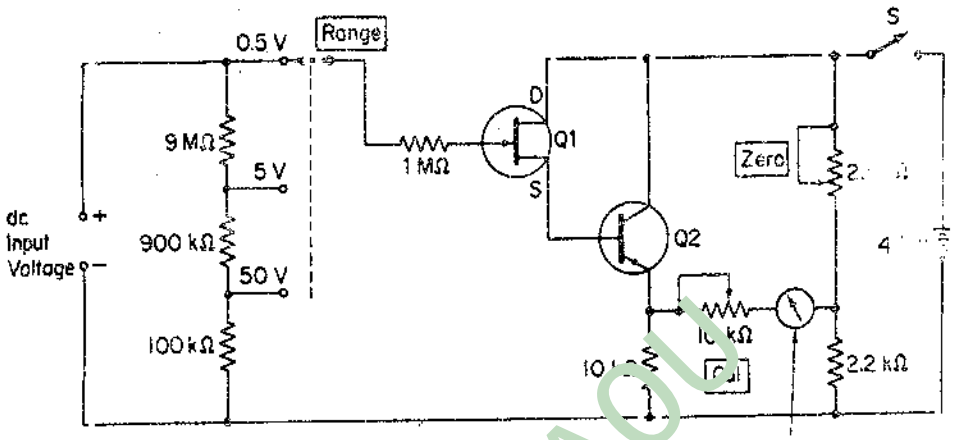


Figure 18.8 Electronic Voltmeter Circuit with FET input

Because the emitter follower must have some bias current present, the emitter voltage does not go to zero volts with zero input voltage. Thus the other terminal of the meter must be returned to ground, but to a voltage that can be set to be equal to the quiescent point of the emitter-follower output V_e. In many practical meters this is made adjustable from the front panel of the meter.

Because the setting of the Zero control affects the total resistance in series with the meter, a Cal (calibrate) control is also supplied. This control is not necessary for amplified meters using a differential amplifier because there is no interaction between the zero adjustment and the calibration of the meter.

18.10 DIFFERENTIAL AMPLIFIER BALANCED BRIDGE TYPE OF ELECTRONIC VOLTMETER

One of the most versatile general-purpose measuring instruments capable of measuring dc and ac voltages as well as current and resistance is the solid-state electronic multi-meter or VOM. Although circuit details will vary from one instrument to the next, an electronic multi-meter generally contains the following elements:

(a) Balanced-bridge dc amplifier and indicating meter

(b) Input attenuator or RANGE switch, to limit the magnitude of the input voltage to the desired value

(c) Rectifier section, to convert an ac input voltage to a proportional dc value (d) Internal battery and additional circuitry, to provide the capability of resistance

measurement

(d) FUNCTION switch, to select the various measurement functions of the instrument such as voltage, current or resistance or DC or AC.

In addition, the instrument generally has a built-in power supply for ac line operation and, in most cases, one or more batteries for operation as a portable test instrument.

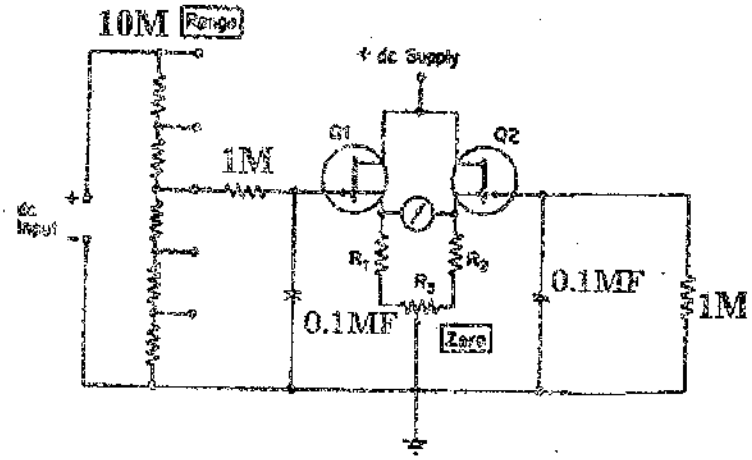


Figure 18.9 Balanced-bridge DC amplifiers with input attenuator and indicating mater

The schematic diagram of a balanced-bridge dc amplifier using field effect transistors or FET's is shown in Fig. 18.2 This circuit also applies to a bridge amplifier with ordinary bipolar transistors or BJT's. The circuit shown here consists of two balanced FET's which sould be reasonably well matched for current gain to ensure thermal stability of the circuit. The two FET's form two upper arms of a bridge circuit. Source resistors R_1 and R_2, together with ZERO adjust resistor R_3, form the lower bridge arms. The meter movement is connected between the source terminals of the FET's, representing two opposite corners of the bridge.

Without an input signal, the gate terminals of both the FET's are at ground potential and the transistors operate under identical quiescent conditions. In this case, the bridge is balanced and the meter indication is zero. In practice, however, small differences in the operating characteristics of the transistors, and slight tolerance differences in the various resistors, cause a certain amount of unbalance in the drain currents, and the meter shows a small deflection from zero. To return the meter to zero, the circuit is balanced by ZERO adjust control R_3 for a true null indication.

When a positive voltage is applied to the gate of input transistor Q_1, its drain current increases which causes the voltage at the source terminal to rise. The resulting unbalance between the Q_1 and Q_2 source voltages is indicated by the meter movement, whose scale is calibrated to agree with the magnitude of the applied input voltage.

The maximum voltage that can be applied to the gate of Q_1 is determined by the operating range of FET and is usually on the order of a few volts. The range of input voltages can easily be extended by an input attenuator or RANGE switch, as shown in Fig. 18.9. The unknown dc input voltage is applied through a large resistor in the probe body to a resistive voltage divider.

The potential divider network in the range selector is designed with a very high total resistance of 10MΩ. Further, a series resistance of 1 MΩ is also included in the gate input terminal, which minimises the loading on the input signal source.

By appropriately modifying the circuit we can measure AC voltages, currents and resistances.

18.11 SUMMARY

The design of both passive d'Arsonval type measuring instruments and instrument like to electronic measuring instruments are studied in the unit. Study of thisunit introduces the student to the field of measuring instruments.

18.12 MODEL EXAMINATION QUESTIONS

1. Give the design consideration to be for converting a d'Arsonva type PMMC mete into Ammeter give the circuit diagram.
2. Give the design consideration to bc for converting a d'Arsonva type PMMC mete into Voltmeter give the circuit diagram.
3. Give the design consideration to be for converting a d'Arsonva type PMMC mete into Ohmmeter give the circuit diagram.
4. How an electronic voltmeter can be designed using FET's ?
5. In what respects to differential configuration in the FET type instrument is better than the other meters.

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18.14 GLOSSARY

PMMC	permanent magnet morrie coil
d'Arsonva	the name of the scientist who design to PMMC
Multiphase resistance	used for converting a current meter into voltmeter
Shut resistance	used for convert to DA ammeter into an ammeter

UNIT – 19: DIGITAL MESURING INSTRUMENTS

Contents:

19.0 AIMS AND OBJECTIVES

This unit introduces you to the principles involved in the design of different types of Digital voltages live simple leaner ramp, staircase ramp, dhal slop successive approximation types.

They will also be introduced the technique of digital frequency counter.

19.1 INTRODUCTION

All analog measuring instruments are being replaced by digital instruments. Hence on emphasis has also been given to the design principles of digital instruments.

19.2 DIGITAL VOLTMETERS AND CLASSIFICATION

The digital voltmeter (DVM) displays measurements of dc or ac voltages as numerals instead of a pointer deflection on a continuous scale as in analog devices. They reduce human reading errors, interpolation errors, eliminates parallax error, increases reading speed, and often provides outputs for further, processing or recording.

The DVM is a versatile and accurate instrument with the developments in integrated circuit (IC) modules, the size, power requirements, and cost of the DVM have been drastically reduced. The DVMs outstanding qualities can best be illustrated by quoting some typical operating and performance characteristics. Such as

(a) Input range: from ±1.000000 V to ±1,000.000 V. with automatic range selection and polarity and overload indication

(b) Absolute accuracy: as high as ±0.005 per cent of the reading
(c) Stability: Very high short-term, 0.002 per cent of the reading for a 24-hr period; (d) Resolution: Very high 1 part in 10^6 (1 μ V can be read on the 1-V input range)

(e) Input characteristics: input resistance ≈ 10 MΩ input capacitance ≈ 40 pF

(f) Calibration: internal calibration stabilized reference source allows calibration independent of the measuring circuit.

(g) Output signals: print command allows output to printer; BCD (binary coded-decimal) output also available for digital processing or recording

Optional features include additional circuitry to measure current and resistance

Digital voltmeters can be classified according to the following broad categories:

(a) Ramp-type DVM – Linear Ramp and Staircase Ramp.
(b) Integrating DVM – Single slope and dual slope
(c) Continuous-balance DVM
(d) Successive-approximation DVM – Digital multimeters.

19.3 LINEAR RAMP-TYPE DVM

The principle of operation of the ramp-type DVM is based on the measurement of the time it takes for a linear ramp voltage to rise from 0 V to the Level of the Input Voltage, or to decrease from the Level of the Input Voltage to 0 V. This time interval is measured with an electronic time-interval counter, and the count is displayed as a number on digital display.

Conversion from a voltage to a time interval is illustrated by the waveforms in Fig. 19.1. At the start of the measurement cycle, a ramp voltage is initiated; this voltage can be positive going or negative-going ramp shown in Fig 19.1 is continuously compared with the known input voltage. At the instant that the ramp voltage equals the unknown voltage, a coincidence circuit, or comparator, generates a pulse, which opens a gate.

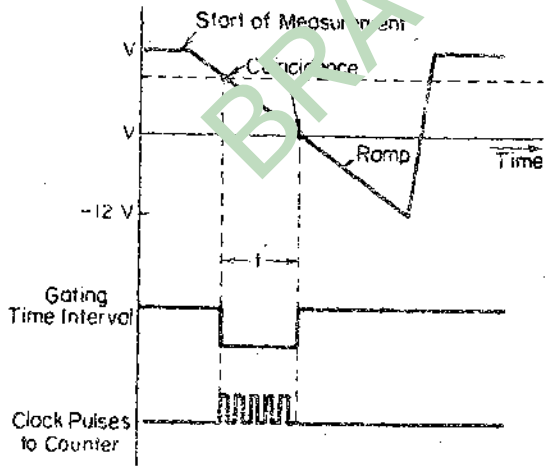

Figure 19.1 Voltage-to-time conversion using gated clock pulses.

This gate is shown in the block diagram of Fig. 19.2. The ramp voltage continues to decrease with time until it finally reaches 0 V (or ground potential) and a second comparator generates an output pulse which closes the gate.

An oscillator generates clock pulses, which are allowed to pass through the gate to a number of decade counting units (DCUs). The number of pulses passed through the gate are displayed by digital display. A sample-rate multivibrator determines the rate at which the measurement cycles are initiated.

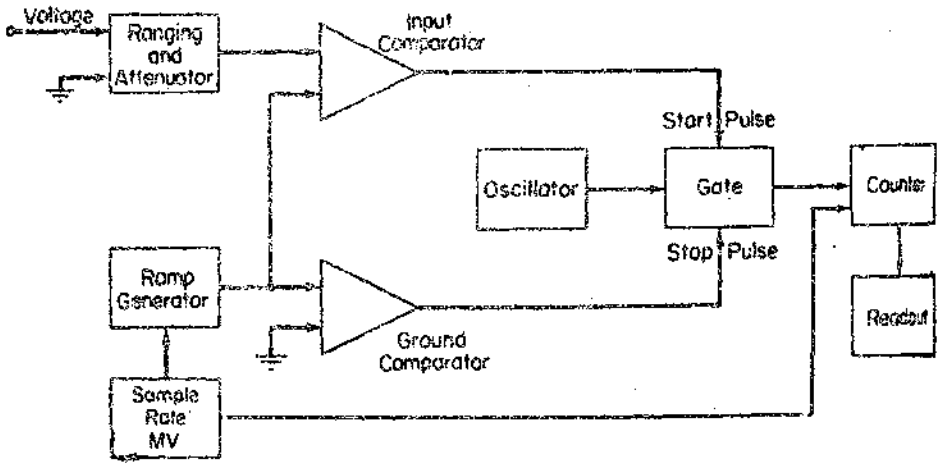

Figure 19.2 Block Diagram of ramp-type digital voltmeter

The sample-rate circuit provides an initiating pulse for the ramp generator to start its next ramp voltage. At the same time, a reset pulse is generated which returns all the DCUs to their 0 state.

19.4 STAIRCASE-RAMP DVM

The block diagram of staircase-ramp DVM is shown Fig. 19.3. It is a modified from of the ramp-type DVM but is somewhat simpler in overall design. Hence it is moderately priced.

This DVM makes voltage measurements by comparing the input voltage with an internally generated staircase-ramp voltage. The instrument shown in Fig. 19.3 contains a 10-M Ω input attenuator, providing five input ranges from 100 mV to 1,00 KV full scale. The dc amplifier, with a fixed gain of 100, delivers 10 V to the comparator at any of the full-scale voltage settings of the input potential divider. The comparator senses coincidence between the amplified input voltage and the staircase-ramp voltage, which is generated as the measurement proceeds through the cycle.

When the measurement cycle is first initiated, the clock (a 4.5-kHz relaxation oscillator) provides pulses to three DCUs in cascade. The over range circuit causes a front panel indicator to light up that the input capacity of the instrument has been exceeded. In advanced versions of DVMs, automatic range and polarity selection is also provided.

The outputs of the D/A converters are connected in parallel and provide an output current proportional to the present count of the DCUs. The staircase case amplifiers convert the D/A current into a staircase voltage, which is applied to the comparator. When the comparator senses coincidence of the input voltage and the staircase voltage, it provides a trigger pulse to stop the oscillator. The present content of the counter is then proportional to the magnitude of the input voltage.

The sample rate is controlled by a simple relaxation oscillator. This oscillator triggers and resets the transfer amplifier at a rate of two samples per second. The transfer amplifier provides a pulse that transfers the information stored in the decade counters to the front panel display unit. The trailing edge of this pulse triggers the reset amplifier which sets the decade counters to zero and initiates a new measurement cycle by starting the clock pulse generator.

The display circuits store each reading until a new reading is completed, eliminating any blinking during the computation.

The disadvantages associated with the ramp type of analog to digital (A/D) converter requires a precision ramp to achieve accuracy. This requires a precision, stable capacitor and resistor in the integrator. In addition, the offset voltages and currents of the operational amplifier used in the integrator are critical in the accurate ramp generator.

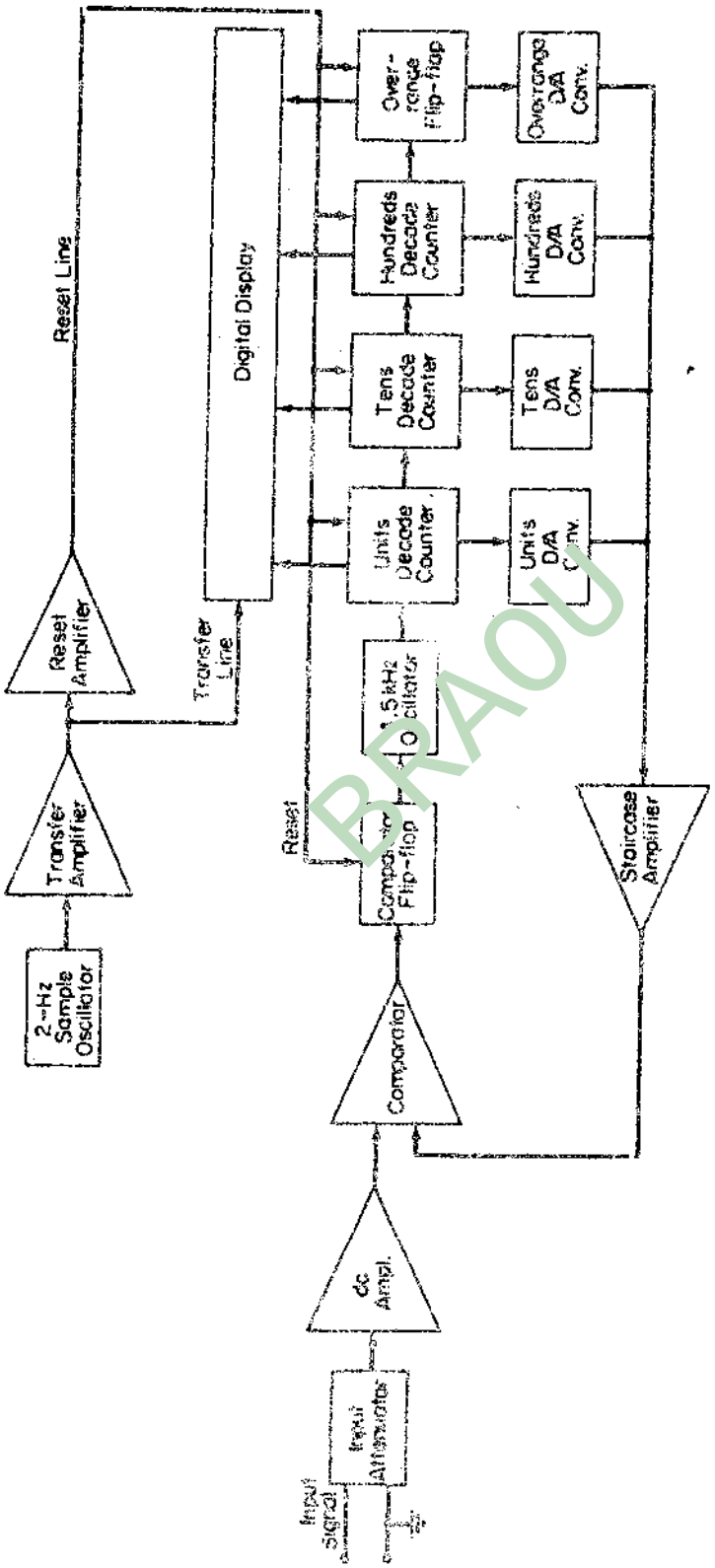

Fig.19.3. Stair Case Ramp DVM

19.5 DUAL SLOPE DVM

One method of reducing the dependence of the accuracy of the conversion on the resistor capacitor and operational amplifier is to use a technique called the dual-slope converter.

In the dual-slope technique, an integrator is used to integrate an accurate reference voltage for a fixed period of time. The same integrator is then used to integrate with the reverse slope, the input voltage, and the time required to return to the starting voltage is measured.

It does not matter which of the two integrations occurs first, and for easy understanding, the unknown voltage is integrated first and then the reference will be considered voltage is integrated next.

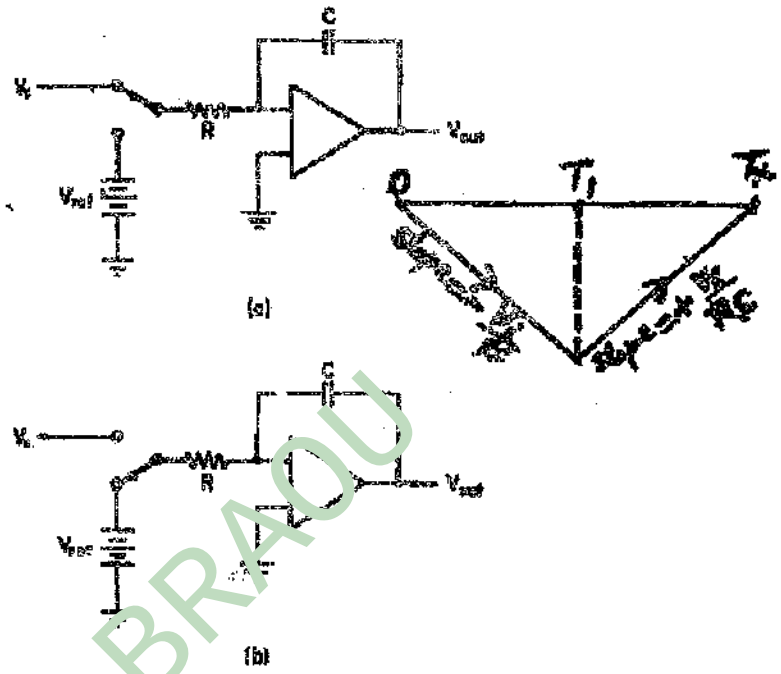

Fig. 19.4 Functional schematic of the integrator of an integrating DVM

The output of an integrator shown in Fig.19.4 (a) is

$$V_{out} = \frac{V_X t}{RC} \qquad \ldots (19.1)$$

where V_X = steady input voltage relative to ground

V_{out}=the output voltage from the integrator

R, C = integrator time-constant components

t = elapsed time from when the integration began

Equation (19.1) also assumes that the integrato capacitor started with no charge and thus the output of the integrator started at zero volts.

If the integration were allowed to continue for a fixed period of time T_1, the output voltage would be

$$V_1 = \frac{V_X}{RC} T_1 \qquad \ldots (19.2)$$

Notice that the integrator output has gone in the opposite polarity to the input. That is, a positive input voltage produces a negative integrator output.

If a reference voltage, V_{ref}, were substituted for the input voltage V_X, as shown in Fig. 19.3, the integrator would begin to ramp toward zero at a rate of (V_{ref}/RC) assuming that the reference voltage was of the opposite polarity as the unknown input voltage. The integrator for this situation does not start at zero but at an output voltage of V_1 and the output voltage can be represented as

$$V_{out} = V_1 + \frac{V_{ref}}{RC} t = V_1 + \frac{V_{ref}}{RC} T_X \qquad \ldots (19.3)$$

Notice that the second term in Equ. (19.4) has a negative sign due to its polarity. Setting the output voltage of the integrator to zero and solving for V_X yields

$$V_X = \frac{T_X}{T_1} V_{ref} \qquad \ldots (19.4)$$

where T_X is the time required to ramp down from the output level of V_1 to zero volts.

Notice that the relationship between the reference voltage and the input voltage does not include R or C of the integrator but only the relationship between the two time intervals relationship between the two times is a ratio, an accurate clock is not required. Further, the disadvantage associated with single slope instrument is eliminated.

Because the integrator responds to the average of the input, it is not necessary to provide a sample and hold. Although the integrator output will not be a linear ramp, the integration will represent the end value by equal to the average of the unknown input voltage. Therefore, the dual-slope analog-to-digital conversion will produce a value equal to the average of the unknown input. Since it does not require a sample and hold circuit, it is cheaper.

The dual-slope method is slow but is quite adequate for a digital voltmeter used for laboratory measurements.

One significant enhancement made to the dual-slope converter is automatic zero correction. As with any analog system, amplifier offset voltages, offset currents, and bias currents the leakage current of the capacitor can cause in the dual-slope A/D converter, will manifest themselves as a reading of the DVM when no input voltage is present.

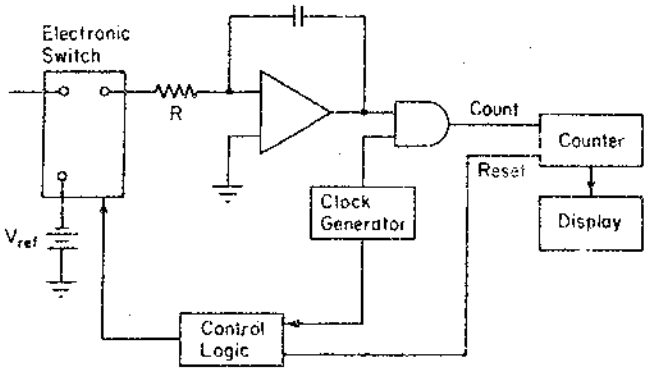

Figure 19.5 shows a complete dual-slope A/D converter. Electronic Integrator C

Figure 19.5 show a complete dual-slope A/D converter. Electronic switches, usually FET switches, are used to switch the input of the integrator alternately between the reference voltage and the unknown. Another pair of switches apply the integrator output to the

automatic zero capacitor and ground the input for the automatic zero function. All of the switch timing and the counting of the clock pulses to determine the unknown voltage are monitored by of the control logic. The output is made available to the external electronics after the conversion is complete.

If, in this example, the reference voltage were 1.000 V and the integrator were allowed to integrate the reference for 1,000 counts, the display would read 1 V full scale with a resolution of 1 mV. The actual frequency of the clock is not critical, as previously explained, but has an effect on the speed of the conversion. As an example, a 10-kHz clock would allow a maximum conversion time of 0.2 s for the example described above.

19.6 SUCCESSIVE-APPROXIMATION (SAR) CONVERSION

A very effective and relatively cheaper method of analog-to-digital conversion is the method of successive approximation. This is an electronic implementation of a technique called binary regression.

Assume that one is to determine the value of a number and is allowed to make estimates. Each estimate would be evaluated and it would be known if the estimate is equal to or less than or greater than the number to be determined. The maximum and minimum value of the possible number is also known.

Consider, as an example, that a number to be determined is between 0 and 511. The best first guess would be some number midway between the extremes and, ideally, 256. To further the example, assume that the number to be determined is 499. The number is greater than the estimate of 256 and this information is provided. It is now known that the number to be determined is between 256 and 511, and, again, something midway makes the most sense for a guess, which is 384. The number to be determined is greater than this estimate, and the next range of estimates is from 384 to 511 for which the midpoint is 448. The number is larger than this and the next range of possible numbers is from 448 to 511, with a midpoint of 480. The number is larger than this, leaving the next range of possibilities from 480 to 511 with the midpoint guess of 496. Again the number is larger and the next range is from 496 to 511, with a midpoint guess of 504. For the time the unknown number is smaller and the range for the next estimate is 496 to 504 with a midpoint of 500.

The number is smaller than this estimate leaving a range of possibilities from 496 to 500. The result of the midpoint guess 498 is the unknown number is greater. The last possible range is from 498 to with a midpoint of 499. This is the ninth estimate and it is known that the number is less than 500 from the seventh guess and greater than 498 from the

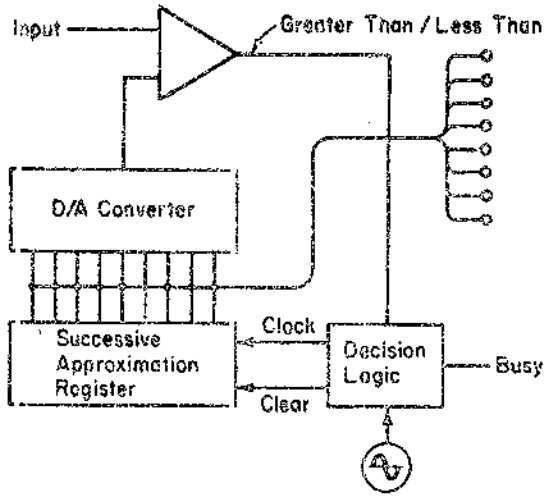

Fig 19.6 Block Diagram of a Successive – approximation DVM

results of eighth guess, and therefore, the number has to be 499. A tabular synopsis of guesses and the results follows.

This continues to all the states until the conversion is complete output assumes the logic one state.

This sequence of events performs, electronically, the same estimating procedure that was outlined previously. An estimate is made on the edge of the SAR clock. For an N-bit conversion after N clocks, the actual value of the input ii known. The least significant bit is the state of the comparator. In some systems an additional clock is used to sort the last bit in the SAR and thus N+1 clocks are required for a conversion.

19.7 SIMPLE FREQUENCY COUNTER

Standards of time and frequency (time and frequency being essentially the same standard) are unique in that they may be transmitted by radio from one location to another without the actual movement of the standard. Therefore, it is possible to have traceability to the primary standard without difficulty. Additionally, the primary standard is related to the structure of matter, and primary standards can be easily duplicated throughout the world to allow high-accuracy measurements anywhere. Because of the relative ease with which frequency and time can be measured to great accuracies, electronics systems have developed around this capability. Consider, as an example, the tolerance expected of radio-transmission equipment. The spectrum required by a voice-modulated two-wa" radio transmitter using frequency modulation is on the order of 15 kHz. This implies that if the frequency of the transmitter carrier could be held to absolute precision a communications channel could be assigned every 15 KHz and make the most efficient use of the radio spectrum. Because accurate measurement techniques are available and standards can be made available, the communications channels are assigned every 20 KHz in the UHF (450 MHz) band. This requires a carrier frequency accuracy and stability of only 5 KHz, which is approximately 0.001 percent, which is easily achieved with modern frequency control and measurement techniques.

Although relatively stable frequency standards have been available for many years, precise frequency measurement has not always been an easy measurement task. Early frequency measurement required precision standards, frequency comparators and interpolation oscillators, as well as a lot of operator skill. This came to an abrupt end with the introduction of digital logic and the development of the frequency counter.

Figure 19.7 shows the block diagram of a simple frequency counter. Although referred to as "simple," this basic counter is capable of great precision if the parts are constructed properly. The frequency counter operates on the principle of gating the input frequency into the counter for a predetermined time. As an example, if an unknown frequency were gated into the counter for an exact I second (s), the number of counts allowed into the counter would be precisely the frequency of the input. The term gated stems from the fact that an AND or an OR gate is used to allow the unknown input into the counter to be accumulated. Figure 19.7 shows the waveforms associated with this action. This example shows an AND gate; however, an OR gate could be used in a similar circuit. A positive-going pulse having a period of exactly I s is applied to one input of the AND gate. As long as the 1-s pulse is a logic I, the output of the AND gate is the same as the unknown input. When the 1-s pulse returns to logic 0, the output of the AND gate is zero. Thus, exactly 1 s of unknown input pulses is allowed at the output of the AND gate. It is necessary to count these pulses and display the result.

If the gate is open for exactly 1 s, the count accumulated is equal to the average frequency of the unknown input in hertz (Hz). If, as an example, the gate was open for 10 s, the accumulated count would be the average frequency in 0.1 Hz. Likewise, if the gate were

open for 0.1 s, the count would be the average

The signal conditioning circuit consists of an attenuator- amplifier - Schmitt trigger system. It offers high impedance to the input signal source. After necessary attenuation amplification, the signal is shaped into a form and amplitude compatible with the rest of the circuit. The conditioned input signal constitutes one of the inputs to the gate.

The time base crystal controlled oscillator produces 1 MHz signal, which is conditioned by the Schmitt trigger. The conditioned 1 MHz signal is processed by a chain of divide-by-ten circuits providing gating times in the range $1\,\mu s - 1s$. When the time base selector switch is is position, it clocks the FF once every second. As a result, the Q output of the FF is alternately HI and LO for 1 second

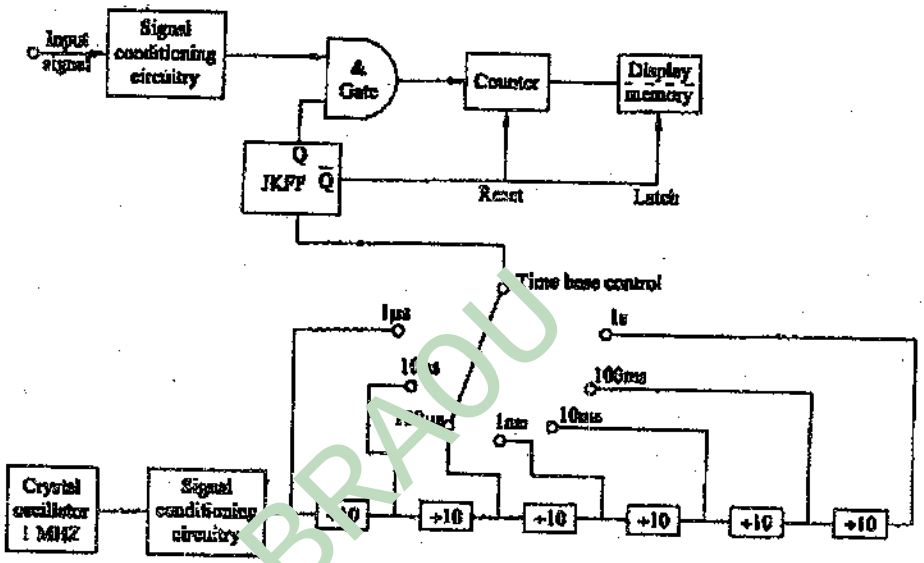

Fig 19.7 Block Diagram of a digital Frequency Meter

When the Q output is HI, the gate is opened. As a result the counter counts for 1 second. At the end of 1-second count period, the Q output goes LO, thus disabling the gate.

The Q output, which is complementary to Q is utilised to reset the counter. The $\overline{Q}$ output goes high when Q goes LO. This triggers a monostable multivibrator whose output is used to latch the next information to the counter. It is also utilised to reset the counter. Then the counter is ready to begin the next count cycle.

19.8 SUMMARY

Design considerations of all types of digital voltmeter as digital frequency meters are thoroughly discussed with complete mathematical background

19.9 MODEL EXAMINATION QUESTIONS

1. Give the circuits diagram and design of linear ramp type digital voltage .
2. What is the advantages of stair case type of ramp over linear ramp.
3. Give the principles and working of a dual slope DVM.
4. What is the disadvantage associate with single slope DVM? How is it over come in dual slope.

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19.11 GLOSSARY

Ramp Voltage	: linearly increasing voltage
Stair Case Ramp	: Step wise increasing voltage

UNIT -20 FUNCTIONING OF CATHODE RAY OSCILLOSCOPE

Contents:

20.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of CRO and make you understand the

1) Essential parts of a general purpose Cathode Ray Oscilloscope

2) Components of Cathode Ray Tube and focusing of electron beam

3) Different types of amplifiers used in C.R.O.

4) Sweep generator and

5) Synchronization circuits

6) Applications of CRO in measurements

After following this unit you will be able to explain the

1. Principle and working of the CRO and

2. Use of various circuits involved in the construction of CRO

20.1 INTRODUCTION

Cathode ray oscilloscope is a versatile testing and measuring instrument with an extensive range of applications covering practically every branch of Science and Technology. It can display rapidly changing electrical quantities. It can be used for the measurement of voltage, current, phase, and frequency in detail.

Mainly this consists of one cathode ray tube and some important electronic circuits like Amplifiers sweep generators, synchronizers etc.

20.2 BASIC CRO OPERATION

The major sub-systems of a general-purpose oscilloscope are shown in simplified block diagram of Fig. 20.1.

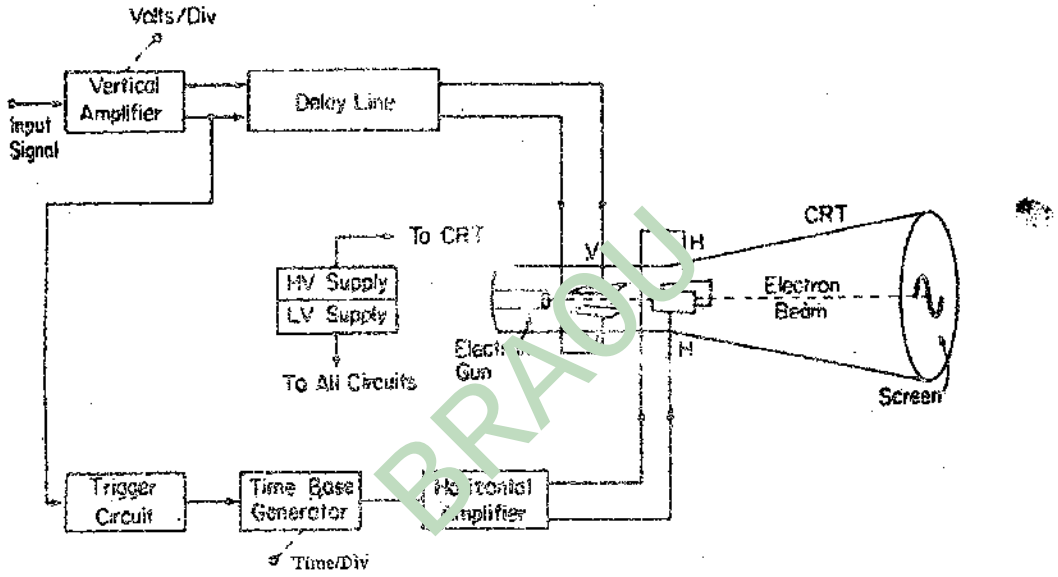

Fig. 20.1 Block diagram of the general purpose CRO

VA-Vertical Amplifier	PS-Power Supply
CRT-Cathode Ray Tube	TC-Trigger Circuit
TBG-Time Base Generator	HA-Horizontal Amplifier
S-Screen	EG-Electron Gun
EB-Electron Beam	H, H-Horizontal Plates
V, V - Vertical Plates	IS-Input Signal

The electron gun, consisting of the cathode, grid and two anodes for accelerating and focusing produce a beam of electrons focused on to the fluorescent screen of the CRT. The point at which the electron beam hits the screen will appear as a bright spot due to fluorescence. Thus the invisible stream of electrons can be visualised on the screen of the tube as a luminous spot. The electron beam, before it strikes the screen, pass in between two sets of plates called X (or horizontal deflection plate) and Y (or vertical) deflection plates. The position of the electron beam (and hence the position of the spot on the screen) can be controlled by applying appropriate voltages to these deflection plates. The voltage, whose time variation has to be displayed is applied to the Y -plates either directly or via an amplifier

called vertical amplifier. The time base or sweep generator produces a voltage, which when applied to X-plates sweeps the electron beam with uniform speed across the tube horizontally providing the necessary time axis. To obtain a stationery picture on the screen, the time base generator is made to operate in synchronism with the output voltage of the vertical amplifier. The output, of the time base generator is also amplified by an amplifier called the horizontal amplifier and then applied to the X-plates. This is a brief description of some important controls of an, 123 oscilloscope. We shall now examine the working of these controls.

20.3 THE CATHODE RAY TUBE

(a) The Electron Gun Assembly

The electron gun, which produces a beam of electrons (see Fig. 20.2), is mounted in the tubular neck of the CRT. The source of electrons is an indirectly heated cathode. The cathode is completely surrounded by a cylindrical electrode called control grid. It has a small aperture at its centre, coaxial with the tube axis. The control grid is maintained at a small negative potential with respect to cathode. This facilitates passing through the grid control of the number of electrons which make up the beam. This in turn controls the brightness of the trace on the screen. The knob on the front panel of the CRO controlling the grid *bias* is known as the intensity or brightness control.

(b) Acceleration and focusing of Electron Beam:

The electrons, emitted by the cathode after passing through the small hole in the control grid, are accelerated by the high positive potential applied to two accelerating anodes.

The three electrodes electrostatic focusing system is shown in diagram of Fig. 18.3. The first electrode of this 'electron lens' is the preaccelerating electrode, a metal cylinder containing several baffles to collimate the electron beam that enters through the small opening on the left-hand side. The second electrode is the focusing anode and the third electrode is the accelerating anode. The preaccelerating anode and the accelerating anode are maintained at a high positive potential (say, + 1500 V). The focusing anode, located between the two accelerating anodes, is connected to a lower positive potential (say, -+ 500 V). Since the field lines are non-uniformly spaced, the equipotential surfaces are curved to form a double concave lens system. This is indicated in Fig. 20.2, by the field lines in the areas between the electrodes. This three electrodes accelerating and focusing system focuses a sharply defined electron beam on to the fluorescent screen

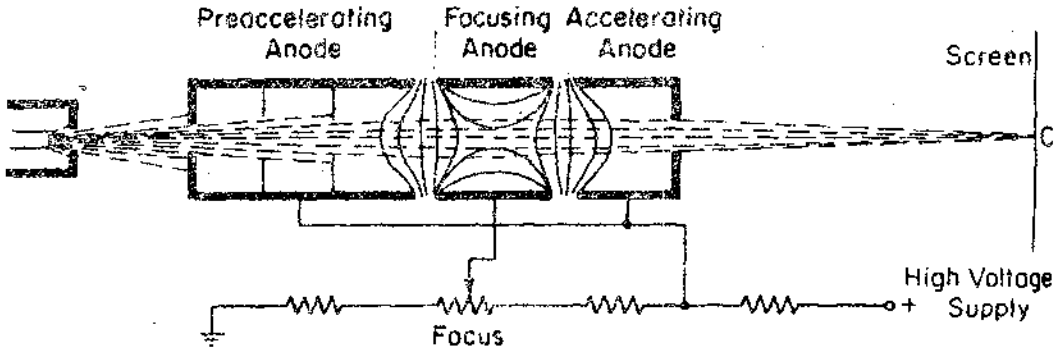

Fig. 20.2. Electrostatic focusing system of a CRT
Al-Pre accelerating Anode F-Focusing Anode

(c) The Deflection System

The accelerated electron beam after passing through the electrostatic lens system passes between two pairs of metal plates: the X-plates or Horizontal deflection plates, which deflect the beam horizontally and the Y-plates or Vertical deflection plates, which deflect the beam vertically. When the plates are uncharged (Fig. 20.4a) the beam of electrons passes through these plates

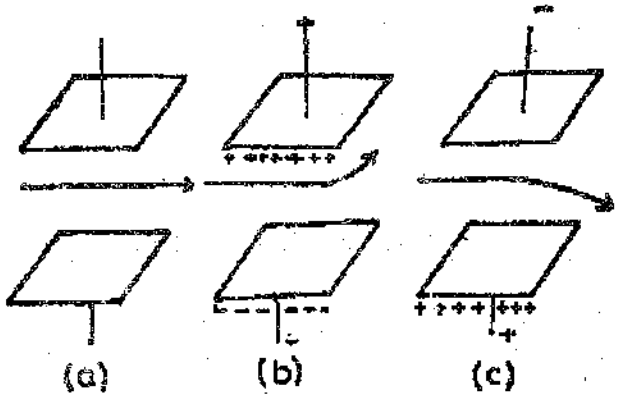

Fig. 20.3 Deflection of the electron beam
(a) No charge on the plates
(b) Upper plate is positively charged with respect to the lower one
(c) Lower plate is positively charged with respect to the upper plate.

without change of direction. Let us see if we connect a battery across one pair of plates, say V-plates, such that the upper plate is positive with respect to the bottom one. Fig.20.4b The positively charged upper plate attracts the negatively charged electron beam, thus deflecting the beam upwards. If the battery terminals are reversed, the beam gets deflected downwardsFig.18.4c The magnitude of deflection is proportional to the voltage applied. A similar but horizontal deflection occurs when the battery is connected to the X-plates. X-and Y shift controls do precisely the same thing as the battery by switching in a D.C. voltage. With these controls the spot can be moved all over the screen by a succession of horizontal and vertical steps.

The horizontal and vertical deflection sensitivity of the CRO is expressed as the voltage needed to deflect the beam, through one cm. In general, oscilloscopes can be switched to different sensitivities (with the help of amplifiers and attenuators) ranging from 10 mV/cm to 100 V/cm.

In order to develop the maximum energy in the electron beam for conversion into visible radiation at the screen, the accelerating voltage must be as high as possible. However, an increase in the accelerating voltage increases the kinetic energy of the electron beam and we need comparatively high voltage at the Y -plates to deflect it. In other words the sensitivity decreases. In ordinary oscilloscopes, a compromise is made between birghtness and sensitivity. A method of achieving a reasonably high sensitivity combined with high intensity is to accelerate the beam after it has passed through the deflecting field, using the so called post deflection accelerator anode or intensifier anode.

(d) The Fluorescent Screen

The inner wall of the wider end of the CRT (the screen) is coated with a phosphor. The phosphor absorbs the kinetic energy of the bombarding electrons and re-emits radiation at a lower frequency in the visible spectrum. The property of some crystalline materials, such as phosphor, or zinc oxide, to emit light when stimulated by radiation is called fluorescence.

Fluorescent materials have a second characteristic, called phosphorescence, which refers to the property of the material to continue light emission even after the source of radiation (in this case the electron beam) is cut off.

20.4 THE VERTICAL AMPLIFIER (Y -AMPLIFIER)

The vertical amplifier should have a large gain of the order of 10^4 - 10^5 since it has to amplify weak signals until they are large enough to cause appreciable deflection of the electron beam. The displayed waveform on the CRT should be an exact representation of the applied signal the amplitude of the signal may vary from a may from fraction of mv to several hundred volts and the frequency may very from few hertz to several mega hertz. For this purpose appropriate attenuator, high gain bandwidth amplifier combination is incorporated between the Y-input terminals and Y plates.

20.5 THE TIME BASE GENERA TOR (SWEEP GENERA TOR)

If an alternating voltage, say 220 V, 50 Hz supply, is applied to the Y -plates without any voltage on the X-plates, the resulting pattern is a vertical straight line. The voltage applied to the Y -plates varies continuously between a positive and a negative peak value and the electron beam follows this continuous variation moving up and down 50 times, a second. Due to the persistence of vision, the pattern appears as a straight line. The length of this line is a measure of the applied peak to peak voltage. To study the voltage variation as a function of time it is necessary to deflect the spot horizontally across the screen at a uniform rate, i.e., we have to provide a time scale along the X direction against which the voltage applied to the Y -plates can be plotted.

20.4 Saw-tooth waveform

This is achieved by applying a saw-tooth wave of the form shown in Fig. 20.4, across the horizontal plates. The saw-tooth wave of the time base voltage is superposed on the direct voltage required for proper centering of the beam.

In a practical RC sweep circuit the switching On and Off is achieved by an electronic switching device, such as a unijunction transistor, a silicon controlled switch, a thyristor, a gas filled triode (thyratron) etc. Fig. 20.6 a shows the UJT relaxation oscillator in which the UJT acts as the switch. When the power is first applied, capacitor C charges exponentially through resistor R and UJT emitter voltage V_{EB1} raises towards the supply voltage

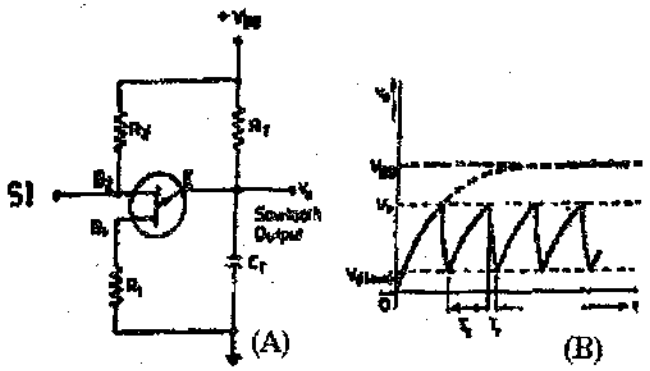

Fig. 20.5 Practical Saw-tooth generator
(a) UJT relaxation Oscillator (b) Output wave - form
SI - SyncInput

V_{BB}. When V_{EBI} reaches the peak voltage V_P of the UJT, the emitter to base 1 of diode becomes forward biased and the UJT triggers on. This provides a low resistance discharge path between E and BI, so that the capacitor discharges rapidly through the UJT. Emitter voltage V' therefore, decreases abruptly until it can no longer sustain the minimum bias required for UJT to remain in E conduction. At this point the low resistance E-B path is broken and the capacitor recharges. This cycle of charging and discharging repeats in a free-running process and produces a saw-tooth waveform as shown in Fig. 20.6b. The repetition frequency of the time base can be controlled by either by varying R or C or both. Coarse frequency control is achieved by switching in different values of C while variation of the charging resistor R constitutes the fine frequency control. The two controls have to be adjusted until a stationary pattern is observed on the screen.

20.6 THE HORIZONTAL AMPLIFIER (X-AMPLIFIER)

The horizontal amplifier magnifies the output of the time base generator before it is fed to the X-plates. The gain of the amplifier controls the length of the sweep on the screen. The internal time base generator is used for the study of time dependent functions. In some applications the vertical signal is displayed as a function of some other signal not linearly related to time; examples are frequency and phase measurements by forming Lissajous figures. In such cases the internal time base generator is disconnected and the relevant external signal is fed to the X-amplifier.

20.7 TRIGGERED SWEEP GENERATOR

In the free running or self-oscillating time base discussed earlier, when the saw-tooth voltage rises to a preset value, the fly back is automatically initiated. The circuit starts generating the next sweep as soon as the voltage reaches its initial value. The time base generates a saw-tooth wave even without any signal at the Y -plates. The initiation of the fly back is controlled by the synchronous (sync) voltage derived from either the Y -amplifier or from an external source. Since the fly back is controlled by synchronous voltage, the later also determines the start of the sweep. This method of synchronizing a free running time base generator external signals is limited in its application to recurrent signals of constant frequency and amplitude.

20.8 SPECIAL OSCILLOSCOPES

In recent times, oscilloscopes with special abilities to deal with complex problems of science and technology have been developed. Some of them are listed below, as the scope of this lesson is limited to introductory quantitative description of the CRO

(a) Dual-beam CRO,

(b) Storage CRO

(c) Sampling CRO

(d) Digital Read out CRO etc.

20.9 LISSAJOUS FIGURES

Construction of the Lissajous Figure

Lissajous figures result when two sine waves are applied simultaneously to horizontal and vertical deflection plates of the CRO.

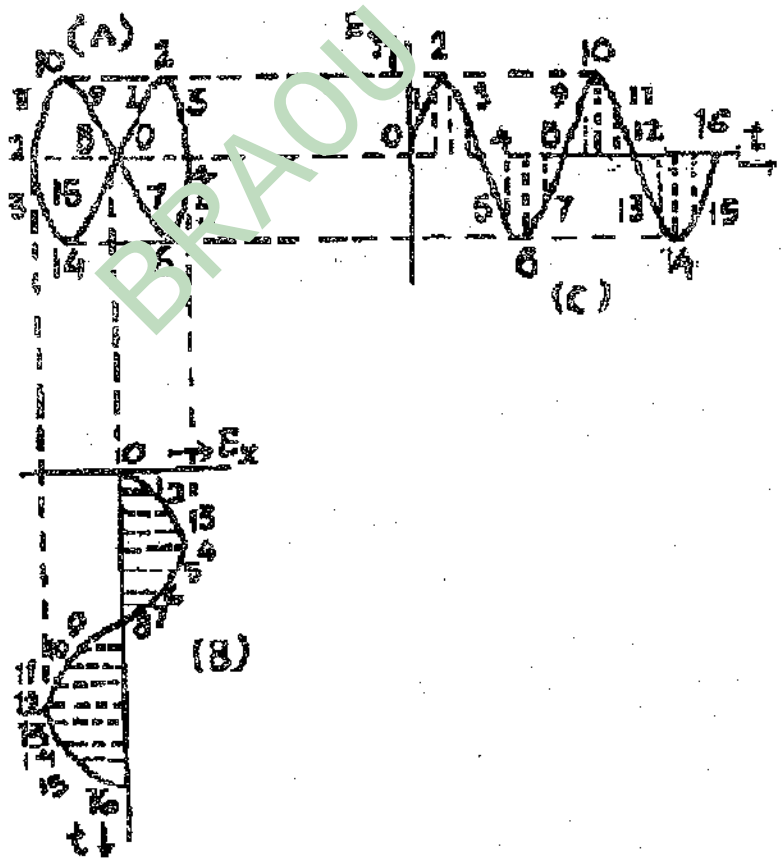

Fig. 20.6 Construction of Lissajous Figure
A-Lissajous Figure B-Horizontal Deflection Voltage (Frequency-F)
C- Vertical Deflection Voltage (Frequency-2F)

The construction of a Lissajous figure is shown graphically in Fig. 20.6 sine wave E_Y represents the vertical deflection voltage and sine wave E_X the horizontal deflection voltage. The frequency of the vertical signal is twice that of the horizontal signal, so that the CRO spot travels two complete cycles in the vertical direction against one cycle in the horizontal direction. Fig. 20.6 shows that numbers 0 to 16 on both the wave forms represent points of corresponding time intervals. Assuming that the spot starts at the centre of the CRO screen (point 0) the movement of the spot can be reconstructed in the manner indicated, and the resultant pattern is called a Lissajous figure.

Two sine waves of the same frequency produce a Lissajous figure, which may be a straight line, an ellipse or a circle depending on the phase and amplitude of the two sine wave signals. A circle can only be formed when the amplitudes of both the signals are equal. If the amplitudes are not equal and or out of phase an ellipse is formed. When the frequencies and amplitudes of signals are equal, the phase difference between the signals determines the type of the pattern formed. Fig. 20.8 shows the phase relationships necessary for each of the pattern produced. An examination of these patterns suggests that one can draw number of conclusions. For example, a straight line results when two signals are either in phase of 180 or out of phase, with each other. The angle formed with the horizontal will be exactly 45° when the amplitudes' of the signals are equal. An increase in the vertical deflection voltage cause the line greater" angle than 45° with horizontal, similarly reduction in vertical amplifier gain results in a line with an angle smaller than 45° with the horizontal. A circle is displayed when the phase difference between the two signals is exactly 90° or 270°, assuming the two signals are equal in amplitude. If the vertical signal has larger amplitude an ellipse with a vertical major axis is formed, when the horizontal signal is larger, the major axis of the ellipse will lie along he horizontal axis.

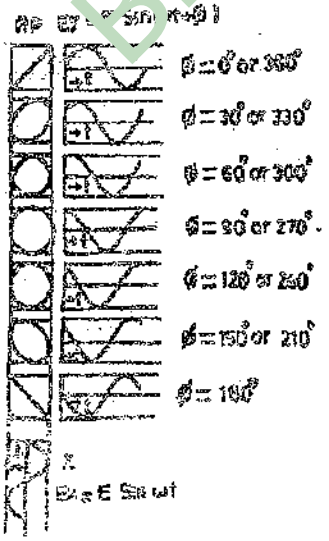

Fig. 20.7 1/1 Lissajous patterns showing the effect of phase relationships
RP- Resulting Pattern X - Horizontal Deflection Voltage
Y - Vertical Deflection Voltage.

In cases of ellipses arising from phase differences other than 90°, a change in relationship between the deflection voltages has the same effect.

20.10 FREQUENCY DETERMINATION

The formation of Lissajous figures when two AC, voltages of different frequencies are superimposed in mutually perpendicular directions may be used for the measurement of frequency. The signal whose frequency is to be measured is given to one set of the plates of CRO, says the Y -plates, and the signal whose frequency is known and is capable of being varied is given to the X-plate of the CRO. The experimental arrangement for the determination of frequency is shown in Fig. 20.8

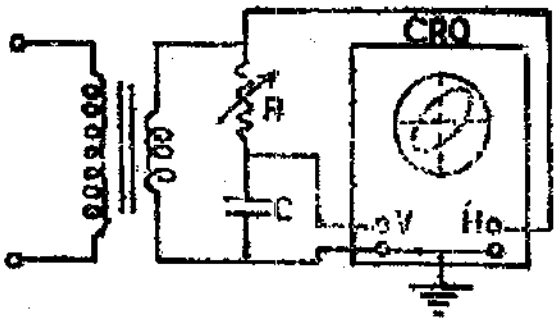

Fig. 20.8 Lissajous figures-experimental arrangement.

Closed-loop Lissajous figures (20.9.) are formed when one of the frequencies is adjusted

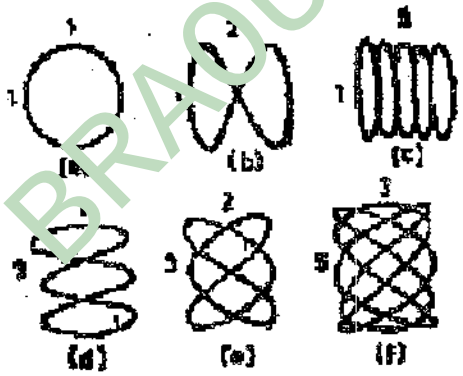

Fig 20.9 Frequency determination - Lissajous figures

such that one frequency is a rational fraction '(or multiple) of the other. The ratio of two frequencies is given by

$$\frac{f_Y}{f_X} = \frac{f_{vertical}}{f_{horizontal}} = \frac{Nuber \text{ of loops which touch the horizontal line}}{\text{Number of loops which touch the vertical line}} \quad \ldots (20.1)$$

There are some restrictions on the frequencies that can be applied to the deflection plates. One, obviously, is that the CRO must have the bandwidth required for these frequencies. The other restriction is that the relationship between the two frequencies should not result in pattern that would be too involved for an accurate determination of the frequency ratio. As a rule, ratios as high as 10/1 and as low as 10/9 can be determined comfortably.

20.11 COMPUTATION OF PHASE ANGLES

Regardless of the relative amplitudes of the 'applied voltages, the ellipse provides a simple means of finding the phase difference between two signals of the same frequency. This method is illustrated in Fig. 20.10. The sine of the phase angle between the two signals is equal tothe ratio of the Y-axis intercept represented by Y_1 to the maximum vertical deflection represented by Y_2 or the ratio of the X axis intercept represented by X1 to the maximum horizontal deflection represented by X_2 We can write

$$\sin\phi = \frac{Y_1}{Y_2} = \frac{X_1}{X_2} \qquad ...(20.2)$$

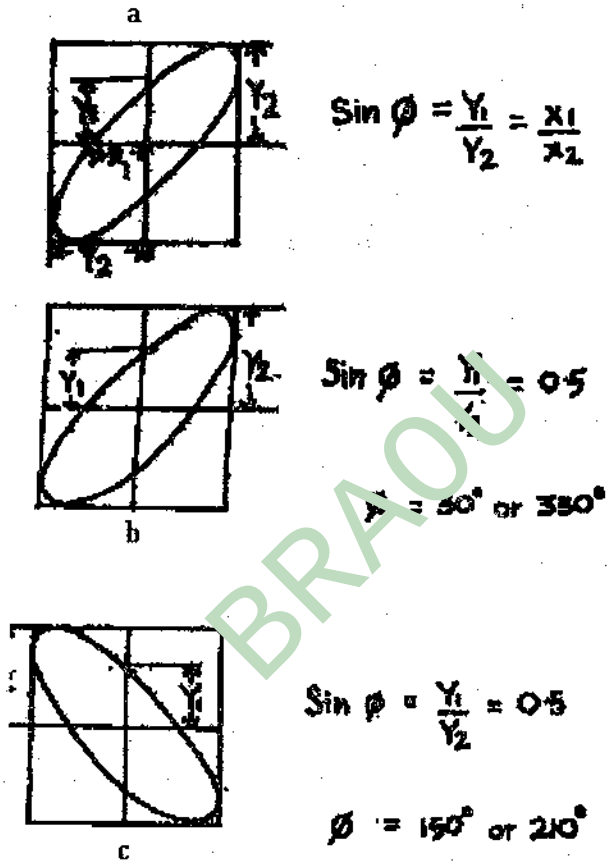

Fig.20.10 Computation of the phase angle between two signals of same frequency

For convenience the gains of vertical and horizontal amplifiers are adjusted so that the ellipse fits exactly within a square marked by the coordinate lines on the graticule. Fig 19.5 shows how to interpret the phase angle corresponding to the orientation of the ellipse. If the major axis lies in the first and third quadrants, as shown in Fig. 20.10 the phase angle is either between 0° and 90° or between 270^0 and 360°. When the major axis passes through the second and fourth quadrants the phase angle is between 90^0 and 180^0 or between 180° and 270°. In the example of Fig. 19.5 the sine of the phase angle equals 0.5, corresponding to different values of phase angles indicated. Fig. 20.11

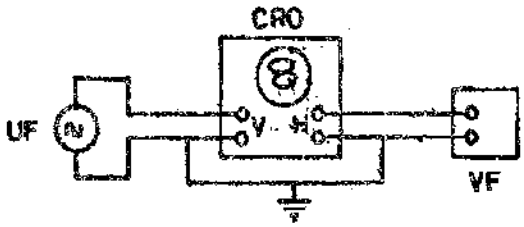

Fig. 20.11 Phase measurements -Lissajous figures
UF - Unknown Frequency, VF - Variable Frequency

indicates the experimental arrangement for the measurement of phase difference between the two signals. The phase angle - can be theoretically evaluated using the relation

$$\phi = \tan^{-1}(\varpi \ R\,C) \qquad \ldots (20.3)$$

where R is the resistance and C, the capacitance used in the circuit shown in Fig 20.9

Reactive elements introduce phase difference between the applied voltage and the resulting current. For example, the current passing through an ideal capacitor leads the voltage across its terminals by 90°. Similarly the current through an ideal inductor lags behind the voltage across its terminals by 90°. The measurement of phase described earlier is one method. Yet there is another method where the waveforms are portrayed on the CRO by applying the two signals one after the other to the vertical input and measuring the shift of an identifiable point of a cycle. Making use of the fact that the distance occupied by one complete wave corresponds to 360° phase, one can evaluate the phase angle.

20.12 SUMMARY

C.R.O. comprises of a cathode ray tube, a fluorescent screen X and Y amplifiers, time base generator Trigger circuit and power supply.

CRO is used in determining the frequency of a sine wave and the phase angle between two sine waves.

20.13 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the block diagram of a general purpose CRO. Label all the blocks and explain the functioning of each block briefly.
2. Describe the various systems in a cathode ray tube.
3. Describe the various systems in a cathode ray tube.
4. Discuss the construction of Lissajous figures with the help of a neat diagram

II. Answer the following questions briefly.

1. Discuss the functioning of time base generator.
2. Write a short note on synchronization.

3. Determination of frequency of an unknown signal.
4. Describe difference between natural sweep and triggered sweep

III. Solve the following problems.

1. A certain Lissajous pattern is produced by applying sinusoidal voltages to the vertical and horizontal terminals of a CRO. The pattern makes five tangencies with the vertical and three with .the horizontal Calculate the frequency of the signal applied to vertical amplifier if the frequency of the horizontal input is 3 KHz [Ans : 5 KHz]

2. A general purpose CRO shows 6em vertical deflection for a signal given to plates of the CRO at a particular given setting. If the horizontal deflection shows 3 em for the same given voltage, evaluate the Vertical gain of the CRO.

20.14 REFERENCES

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20.15 GLOSSARY

Transducer	:	A device which converts one form of energy into another form. If it is possible in the opposite direction then the transducer is called reversible transducer.
Phsopher	:	A substance that is capable of showing energy and later releasing it in the form of light.
Band width	:	The range of frequencies with in which the performance of an amplifier does not differ from its maximum value by a specific amount.

BLOCK – VII

MODULATION AND DEMODULATION

UNIT – 21 AMPLITUDE MODULATION AND DEMODULATION

Contents:

21.0 AIMS AND OBJECTIVES

Now you are going to be introduced to the basic communication systems like Radio and Television. In general Radio Waves are used for the transmission of sound (audio) and Picture (video) signals. Different types of modulations like amplitude, frequency and phase modulation are necessary, for this purpose.

This unit deals with the

1) Process of Amplitude Modulation (AM)

2) Types of Amplitude Modulation and

3) Process of AM Detection

After going through this you will be able to analyse

1) The need for Modulation and Demodulation (Detection)

2) The principles involved in amplitude modulation

21.1 INTRODUCTION AND NEED FOR MODULATION

To carry information from one place to another every transmitting station uses a particular high frequency radio wave called the carrier wave. The information (speech or music or picture) is made to modify any one of the characteristics of the carrier wave. This process of altering the Amplitude or the Frequency or the Phase of the carrier wave in accordance with the signal to be transmitted is called modulation. The modulated wave is decoded or demodulated at the receiving end to separate and extract information from the carrier wave. Anyone of the three characteristics of the carrier wave can be modified to allow

it to "Carry Information". Accordingly we have amplitude modulation (AM), frequency modulation (FM) and the phase modulation (PM). We will discuss amplitude modulation in this unit. Frequency modulation constitutes the subject matter of the next unit.

Why do we modulate the carrier wave at the broadcasting station and then demodulate- it at the receiving station? Can we not transmit speech or music by converting them into corresponding electromagnetic signals (using the microphone and the amplifier) without modulation? There are two difficulties that prevent such direct transmission of very low frequency information signals.

(i) For transmitting the highest voice frequency at 15 KHz the dimensions of the antenna should be $\lambda/4$ = 5000 meters and for transmitting lower frequencies the dimensions should be much greater. On the other hand, if a high frequency carrier wave of 1 MHz frequency is modulated, then the size of the antenna $\lambda/4$ = 75M. If the carrier frequency is further increased the dimensions of the antenna become smaller and are manageable. (where λ= e/f, c-is the velocity of an electromagnetic wave = $3X10^8$ Meter/sec and f is the frequency).

(ii) Human voice generates frequencies in the range 50 Hz to 5 kHz. The corresponding electromagnetic waves lie in the same frequency range. If every transmitting station transmits these frequencies directly, they interfere at the receiving station and cause confusion.

(iii) Efficient transmission and reception at these low frequencies require antennas whose dimensions should be equal to $\lambda/4$ meters. It is not feasible to fabricate such huge antenna systems.

(iv) Different broadcasting stations operating at different carrier frequencies automatically avoid the interference of signals at the receiving station.

21.2 TECHNIQUES OF MODULATION AND DEMODULATION

Several analog and digital modulation and de-modulation techniques are developed for transmission and reception of information signals.

(a) Analog Modulation Techniques

Amplitude Modulation (AM), Frequency Modulation (FM); Phase Modulations (PM) are the three analog techniques by which the modulation and de-modulation are carried out. In these three techniques the first two AM and FM are widely used for radio and TV communications.

(b) Digital Modulation Techniques

Pulse Amplitude Modulation (PAM); Pulse Width (Duration or Time) Modulation (PWM or PDM or PTM); Pulse Position Modulation (PPM) ad Pulse Code Modulation (PCM). These techniques are extensively being used in modern communications of which the PCM is truly digital technique and is the best and most widely used technique.

21.3 AMPLITUDE MODULATION (AM)

Amplitude modulation is the process in which the low frequency signal containing information modifies the amplitude of the carrier wave. The frequency of the carrier wave remains constant. Amplitude modulation is achieved by combining the signal (modulating wave) and the carrier wave using a non-liner device (diode or transistor or FET etc.). The waveforms of the modulating signal, the carrier wave and the modulated wave are shown in

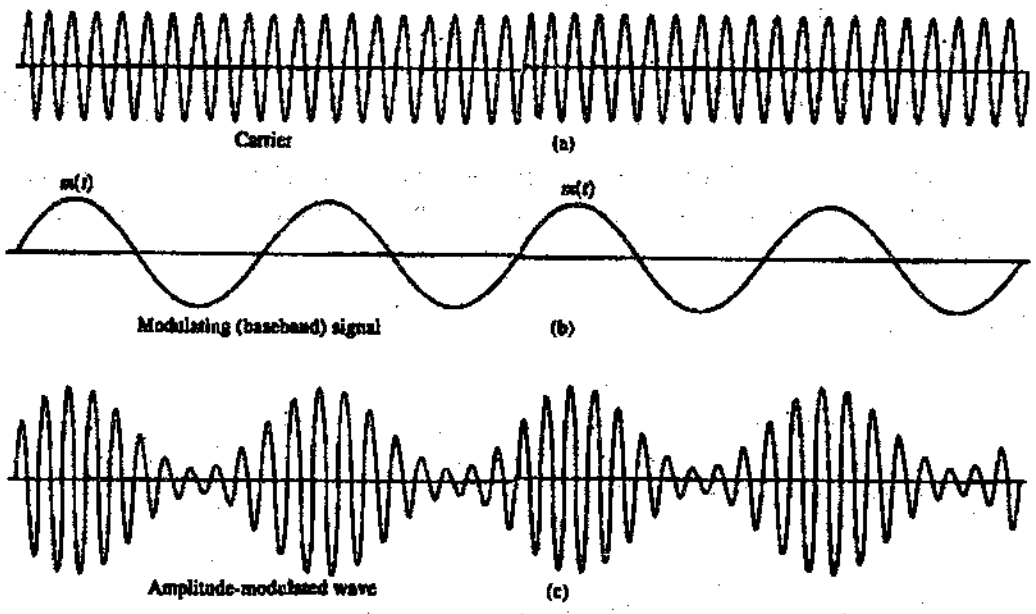

Fig25.1

Fig. 21.1. Amplitude Modulation - Wave forms
(a) Carrier wave (b) Information Signal
(c) Amplitude Modulated Wave

21.4 MATHEMATICAL ANALYSIS OF AM WAVE

The un modulated carrier wave is represented by

$$V_C \sin \varpi_C t = V \sin 2\Pi f_C t \quad \ldots (21.1)$$

Where f_C is the carrier frequency and V_C is the amplitude of the carrier wave. In amplitude modulation f_C remains constant while V_C varied in accordance with the amplitude of the modulating information signal and at the rate as the modulating signal frequency. The modulating information signal is represented by

$$V_S \sin \varpi_S t = V_S \sin 2\Pi f_S t \quad \ldots (21.2)$$

where f_S is the frequency of the information (modulating) signal and V_S is its amplitude. The amplitude of the modulated signal can be expressed as:

$$V_m = (V_c - KV_S \sin \varpi_S t) \sin W_C t \quad \ldots (21.3)$$

where k is a factor that depends on the modulating circuit.

As mentioned earlier. its amplitude varies sinusoidally about a mean value V_C. It has a maximum value of $(V_C + kV_S)$ and a minimum value of $(V_C - kV_S)$ Equation (21.3) may be rewritten as:

$$V_m = V_C \left(1 + \frac{kV_S}{V_C} \sin \varpi_S t\right) \sin \varpi_C t \qquad ...(21.4)$$

$$V_m = V_C(1 + m_a \sin \varpi_S t) \sin \varpi_C t \qquad ...(21.5)$$

The factor $kV_S / V_C = m_a$ is called the modulation factor or modulation index. It may take any value between 0 and 1. When m_a = O. there is no modulation; m_a = 1 indicates 100% modulation. .

Using the trigonometric relation.

$$\text{Sin A Sin B} = 1/2 \text{ Cos (A - B)} - 1/2 \text{ Cos (A + B)}$$

We may expand equation (20.5) in a similar way as

$$V_m = V_C \sin 2\Pi f_C t + \frac{m_a V_C}{2} \text{ Cos } 2\Pi \text{ } (f_C - f_S)t + \frac{m_a V_C}{2} \text{ Cos } 2\Pi \text{ } (f_C + f_S)t \qquad ...(21.6)$$

An examination of the above equation shows that the modulated wave consists of three components:

(i) The carrier frequency f_C

(ii) The upper side frequency $(f_C + f_S)$ and

(iii) The lower side frequency $(f_C - f_S)$

In communications modulation by a single frequency is not used. Several frequencies are simultaneously used. In transmission of voice, the audio signal is very complex as it contains frequencies in the range of 50 Hz – 5 KHz. As mentioned earlier, each signal frequency results in two side frequencies in the modulated wave. Hence, in transmission of complex signals the AM wave contains sidebands instead of side frequencies as shown in Fig. 21.2.

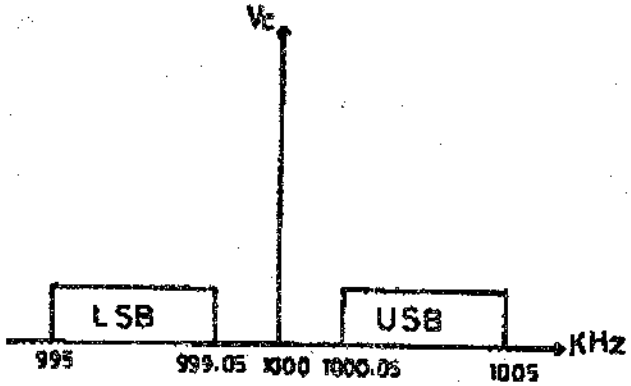

Fig. 21.2. Amplitude modulated signal Frequency Components
LSB - Lower side band
USB - Upper side band

For example a carrier frequency of 1000 kHz and signal frequencies in the range 50 Hz - 5000 Hz leads to a band of frequencies in the range 1000.05 KHz - 1005.00 kHz (upper sideband) and another in the range 995 kHz - 999.05 kHz (lower sideband). Hence, the total

bandwidth required for transmission is 1005.00-995.00 = 10KHz ie double the highest signal frequency to be transmitter.

Experimental determination of Modulation Index:

From fig 21.1(c). It can be seen that

$$V_S = \frac{V_{max} - V_{min}}{2} \text{ and } V_C = \frac{V_{max} + V_{min}}{2} \quad \ldots(21.7)$$

$$\therefore \text{the modulation index } m = \frac{V_S}{V_C} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \quad \ldots(21.8)$$

21.5 POWER RELATIONS

According to equation (21.6) the voltage components (rms values) of the carrier and the side frequencies are $\left[\frac{V_C}{\sqrt{2}}\right], \left[\frac{m_a V_C}{2\sqrt{2}}\right] and \left[\frac{m_a V_C}{2\sqrt{2}}\right]$ respectively. If these components are impressed across a resistor R, the average power is given by

$$Pt = \left[\frac{V_C^2}{2R}\right] + \left[\frac{m_a V_C^2}{8R}\right] + \left[\frac{m_a^2 V_C^2}{8R}\right]$$

$$= \frac{V_c^2}{2R}\left(1 + \frac{m_a^2}{2}\right) = P_C\left(1 + \frac{m_a^2}{2}\right) \quad \ldots(21.9)$$

$= Pc + P_{SB}$

=(Power of the carrier + power of the two sidebands).

Here $\frac{V_c^2}{2R}$ represents the power in the carrier wave and

$\frac{V_C^2 m_a^2}{8R}$ Represents the power in each of the side frequencies.

or $\frac{V_C^2 m_a^2}{4R}$ is total power in both the upper and lower side bands.

With $m_a = 1$, the power content of the modulated wave is 50% greater than that of the carrier wave.

21.6 GENERATION OF AM WAVES

Amplitude modulation is produced by combining the carrier and the information signals using a non-linear device. Diodes are non-linear devices but they are not used. as they do not offer any gain. Transistors behave as non-linear elements and also offer gain. As such they

are suitable for this application.

Fig. 21.3 shows a simple transistor modulator. The carrier frequency signal is inserted the base circuit and modulation signal is coupled either into the emitter circuit or into the collector circuit as shown Fig. 21.3 (A,B) respectively . The coupling of the low frequency information signal is achieved through an audio frequency transformer 'T' as show in the figures.

The amplitudes V_C and Vs are adjusted so as to bias the transistor in the non-linear part of its characteristic. The collector circuit contains a resonant circuit, which is tuned to the carrier frequency. The resonance curve of the tuned circuit should be broad enough to accept the side frequencies also. The modulated wave is taken from the collector circuit as shown in the figure.

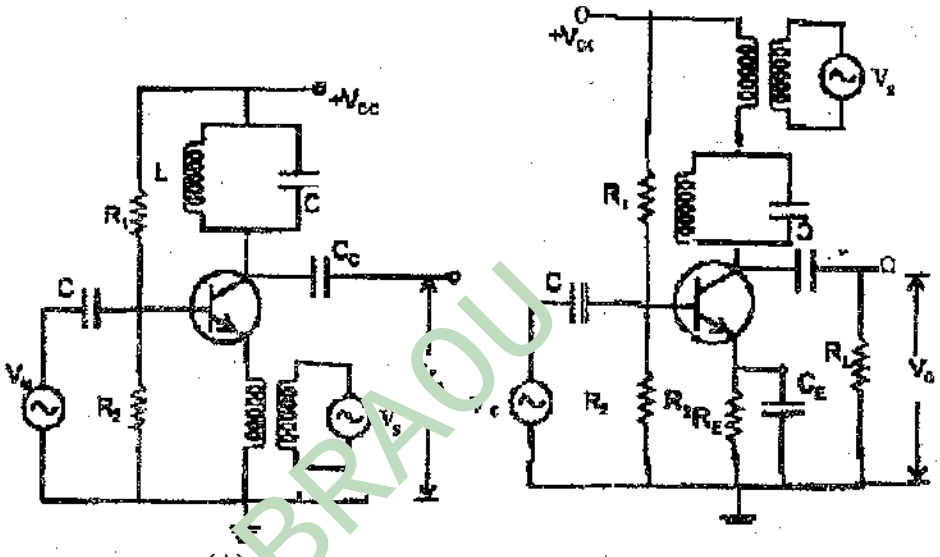

Fig 21.3 Simple Transistor Modulator
V. -Carrier; T-Transistor
V, -Signal; a-Output

21.7 DEMODULATION OR DETECTION OF AM SIGNALS

A simple method for demodulation or detection of amplitude-modulated waves involves rectification of the signal and filtering high frequency carrier (the rf) and rejecting (or blocking) the DC components. The circuit diagram of such a detector is shown in fig. 21.4.

The amplitude-modulated signal is rectified by diode D. The rectified wave is shown at A in the figure, which still contains the HF carrier. The combination $C_1 - R_1 - C_1$ is a low pass filer, which removes the high frequency component and allows only the low frequency information signal superposed over a DC component (this wave form is shown at point B). The dc component is eliminated by a series capacitor C_2 which blocks the DC and clocking allows only the AC component i.e., the information signal.

To avoid distortion of the detected wave we should satisfy the equation

$$R_1C_1 = \frac{1}{\sqrt{\omega_c \omega_s}} \qquad \ldots(21.10)$$

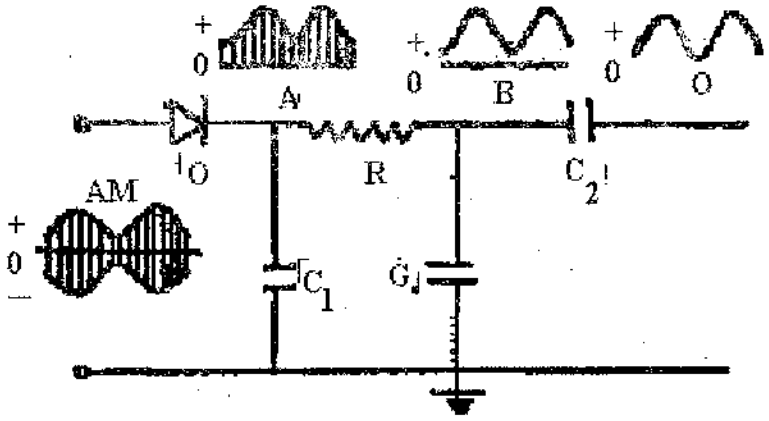

Fig. 21.4 Simple detector AM-Amplitude Modulated Wave

Worked Example -1: An audio signal 15 Sin 2 Π (1500t) amplitude modulates a carrier 60 Sin 2 Π (100000 t). What are the frequencies of the audio signal and the carrier? What are the side frequencies? Determine the modulation factor.

Solution:

(a) The audio signal is represented by 15 sin 2 IT (1500 t) Hence f. = 1500 Hz

(b) The carrier is represented by 60 sin 2 It (100000 t). Hence f. = 100000Hz

(c) Side frequencies are $f_C + f_B$. = 100,000 + 1500 = 101,500 Hz

$f_C - f_B$ = 100 000 - 1500 = 98 500 Hz

(d) Modulation factor $m_a = \frac{V_B}{V_C} = \frac{15}{60} = 0.25$

Worked out Example-2: The total power of an AM signal is 100 W. Determine the power of the carrier and each of the side bands if m = 1.

Solution:

Given Pt = 100 W

$m_a = 1$

$$P_t = P_C \left(1 + \frac{m_a^2}{2}\right)$$

$100 W = P_C + 0.5 P_C = 1.5 P_C$

$$P_C = \frac{100}{1.5} = 66.67 \text{ watts}$$

Power in side the bands = $P_t - P_c$ = 33.33 watts.

$$\text{Power in each side band} = \frac{33.32}{2} = 16.6 \text{ watts}$$

21.8 SUMMARY

Amplitude modulation is a process of modulating a signal for efficient transmission. Modulation index varies from 0-1. Carrier wave can be filtered using the process of demodulation by rectifying the modulated signal.

21.9 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Draw the circuit diagram of amplitude modulator and explain its working,
2. Explain how amplitude modulated waves are detected. Give the necessary diagrams and waveforms.

II. Answer the following questions briefly.

1. Discuss the need for modulation in radio and television transmissions.
2. Distinguish between amplitude and frequency modulation.
3. What are side frequencies? Why do we have side bands?
4. Discuss the power relations between the carrier and side bands in an amplitude-modulated wave.
5. Derive an expression to represent an amplitude-modulated wave.

21.10 REFERENCES

1. Electronic Communication Systems	Kennedy Geroge
2. Communication Sys.	Lathi B.P
3. Modern Digital and Analog Communications	Lathi B.P
4. Electronic Communication Systems	Thomsi
5. Advanced Electronic Communication Sys.	Thomsi Wayne

UNIT-22: FREQUENCY MODULATION AND DEMODULATION

Contents:

22.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

1) Defect in Amplitude Modulation

2) Frequency Modulation and detection

3) Generation of FM Waves

After following this unit you can discuss the

1) Need for frequency modulation

2) Method of analysing a frequency modulated wave

3) Circuits for generation and detection of FM signals

22.1 INTRODUCTION

Amplitude modulated signals are influenced by noise. Most noise appears as additional amplitude modulation on the signal. The effect of noise is minimised in frequency modulation. In frequency modulation the signal is placed on the carrier by varying its frequency while keeping its amplitude constant, shown in Fig. 22.1.The carrier wave has a frequency f_C and an amplitude V_C the modulating signal has a frequency f_S and amplitude V_S. The instantaneous frequency of the modulated wave varies sinusoidally with time above and below its mean value f_C. The number of times per second that the wave goes through a complete cycle frequency variation is equal to f_S. The maximum frequency shift Δf is known as frequency deviation. The value of Δf is given by

$$\Delta f = K_f V_S \qquad \ldots (22.1)$$

where K_f is a parameter that depends on the nature of the circuits employed. It depends on the amplitude of the modulating signal. It does not depend on the frequency of the modulating

signal.

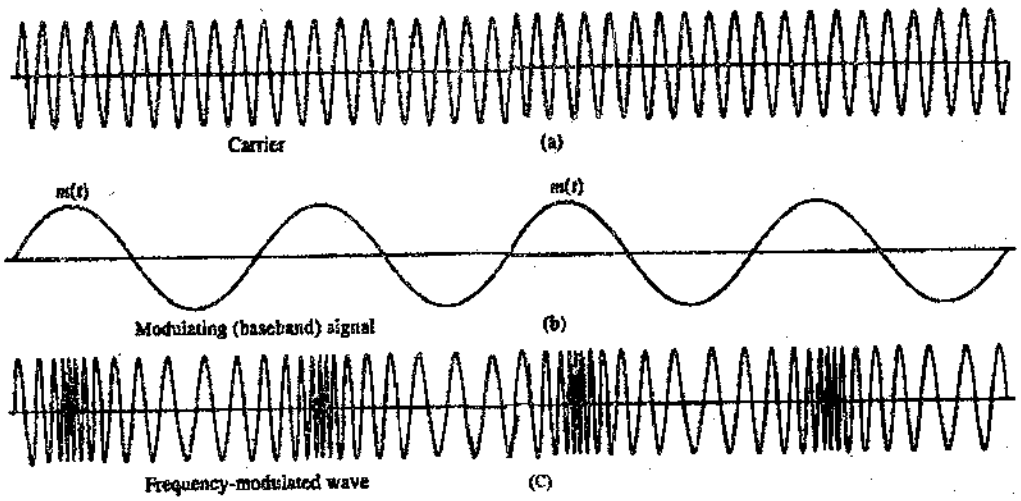

Fig. 22.1 Frequency Modulation
(a) Information(b) FM Wave(c) Frequency Modulated Wave

22.2 ANALYSIS OF FM WAVE

The general expression for an un-modulated carrier wave can be written as

$$v_e = V_C \sin (w_c t \times \phi) \quad \ldots (22.2)$$

Where v_e = the instantaneous value of voltage of the carrier wave.
V_c = Amplitude of the carrier wave.
W_c = Angular frequency rads/sec.
ϕ = Phase angle in rads.

If the modulating signal is also a sine wave, which can be expressed as

$$v_s = V_S \sin (W_S t) \quad \ldots (22.3)$$

In frequency modulation, the amplitude of the carrier wave is maintained constant and the frequency of the carrier is alone varied. Hence, the importance frequency of the frequency of the modulated wave can be expressed as

$$W_m = W_C (1 + K V_S \text{ Cos } W_S t)$$

Or

$$f_m = f_c (1 + K V_S \text{ Cos } W_S t) \quad \ldots (22.4)$$

Hence cosine function has been preferred for simplicity in calculations.

Where f_C - is the un-modulated carrier frequency.
f_m – modulated carrier frequency
k – is a constant
W_S – the circuit employed to modulation.

The maximum deviation in frequency occurs when the cosine term in Equ.22.4 has its maximum

Hence Equ. 21.4 reduces to

$$f_m = f_C (1 \pm K V_S) = f_C \pm K V_S f_C) \quad \ldots (22.5)$$

$$= f_C(1 \pm \delta) = f_C \pm \delta f_C \quad \ldots(22.6)$$

Where the maximum frequency deviation is given by

$$\delta = K V_S f_C \quad \ldots(22.7)$$

From Equ. 21.4, we have

$$W_m = W_C (1+K V_S \text{Cos} W_S t) \quad \ldots(22.8)$$

We have

$$W = \frac{d\theta}{dt}$$

$$d\theta = W dt$$

$$\theta = \int d\theta = \int dt \quad \ldots(22.9)$$

$$= \int W_C(1 + K V_S \text{ Cos } W_S t)dt$$

$$= W_C \left[t + \frac{K V_S \sin W_S t}{W_S} \right]$$

$$= W_C t + \frac{K E_S W_C \text{ Sin } W_S t}{W_S}$$

$$\theta = W_C \left[t + \frac{K V_S f_C \sin W_S t}{W_S} \right] \quad \ldots(22.10)$$

Or

$$\theta = W_C + \frac{\delta}{f_S} \sin W_S t \quad \ldots(22.11)$$

The instantaneous amplitude carrier is given by

$$\ell_{fm} = A \sin \left[W_C t + \frac{\delta}{f_S} \sin W_S t \right] \quad \ldots(22.12)$$

$$m_f = \frac{\text{maximum frequency deviation}}{\text{modulating frequency}} \quad \ldots(22.13)$$

submitting (21.13) in (21.12)

$$\ell_{fm} = A \sin \left[W_C t + \frac{\delta}{f_S} \sin W_S t \right]$$

The description of the FM wave is more complex than the AM wave. The Fm

wave contains large number of side bonds, which can be expressed by a set of tables or canvas known as Bessel Functions. The FM frequency spectrum (carrier and the lower and higher side bonds are shown in Fig 22.14) for low and high values of modulating index)

The value of m_f depends on the amplitude of the modulating signal and upon the signal frequency.

$$V=A \sin\bullet \qquad \ldots (22.14)$$

Analysis of the FM wave shows that unlike the AM wave, which has two side frequencies for, each modulating frequency; it has an infinite number of side frequencies spaced f_s apart as shown in Fig. 22.2.

Fig. 22.2 Components of a FM wave (side bands)

However most of the side frequencies do not contain significant amounts of power. The bandwidth of a FM wave is given by

$$BW = 2nf_s \qquad \ldots(22.15)$$

where n is the number of side frequency pairs of significant amplitude

It may be mentioned that the power of the carrier wave is not changed by modulation. Power in the side bands is derived from the carrier wave.

22.3 A SIMPLE FM GENERATOR

(a) Condenser Microphone FM Generator

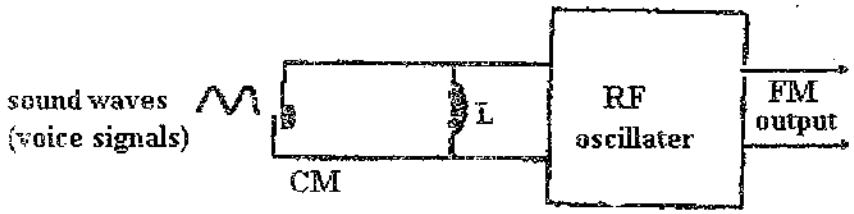

Fig 22.3 simple FM generator
CM- condenser microphone; -Inductance
RFO-Radio frequency Oscillator.

Fig. 22.3 shows the simple circuit that illustrates the process of generating FM waves. It is a radio frequency oscillator having the resonant circuit of its shown in the figure. The capacitance part of the LC is not a conventional condenser, It is a capacitor microphone Without sound waves, the microphone presents a constant value of capacitance and the circuit oscillates at a particular frequency f_c. When sound waves reach the microphone, they produce

vibrations of the diaphragm of the microphone and cause the capacitance to vary. The magnitude of the capacitance change is proportional to the amplitude of the sound wave and the rate of change of capacitance is equal to the frequency of the sound waves. As a consequence, the frequency of the oscillator varies according to, equation (22.5) thus producing FM waves.

(b) Varactor Diode FM Generator:

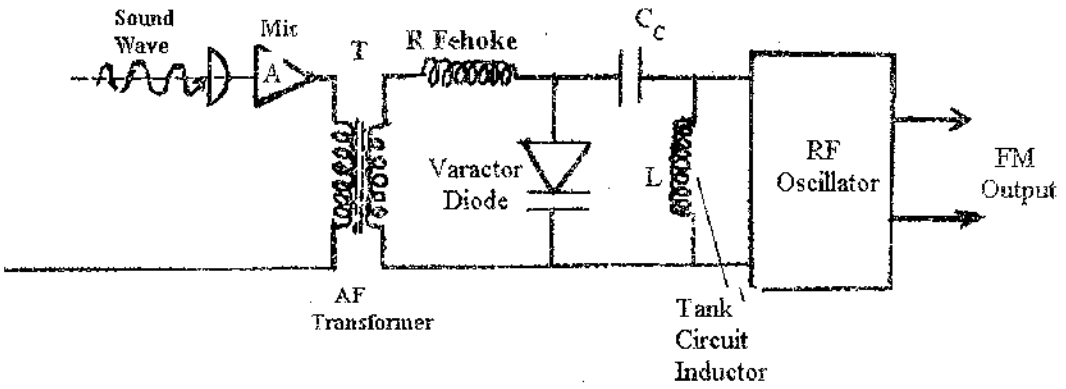

Fig 22.4 Varactor Diode frequency modulator

As mentioned earlier, the circuit shown in Fig. 22.3 only illustrates the principle. Practical circuits are complex and are beyond the scope of this unit.

The sound waves are picked up a microphone and are amplified by an audio frequency amplifier. The AF signal is compiled to the varactor diode the function capacitance of the reverse biased varactor diode is varied by the modulating AF signal. Hence, the resonant frequency of the tank circuit comprising of the varactor diode functioning capacitance C_D and inductance varies. Hence, the RF oscillator frequency also varies thus frequency modulation of the carrier wave is achieved.

In this the RF choke prevents the RF oscillation going into the AF transfer. C_C is a large capacitor, which couples the RF oscillation of the tank circuit to the oscillator but blocks the DC voltage. These two methods are simple and direct methods Reactance modulation of active device like the FET and an indirect method like the Armstrong frequency modulation techniques are available. However, they are highly sophisticated and are beyond the scope of this course.

22.4 FM DETECTION

(a) Slope Detector:

A circuit that produces an output voltage whose amplitude is proportional to the frequency of the input signal can be used to decode or detect FM signals. Such circuits are called frequency discriminators. A simple FM discriminator is shown in Fig. 22.5. It is a radio frequency amplifier, which has a tuned circuit in its input i.e., a tuned amplifier. The LC circuit is detuned. For example, we tune the amplifier to have resonant frequency f_0 above the carrier frequency - f_c. f_c as shown in Fig. 26.4 b. The output of the amplifier will then have amplitude that is proportional to the incoming signal frequency over a limited range.

In view of its limited range the circuit shown in Fig. 22.5 is not used in practice. More sophisticated FM detectors like balanced slope detector, phase discriminator, ratio detector

are employed in practical application. However, they are more complex and are beyond the scope of the course.

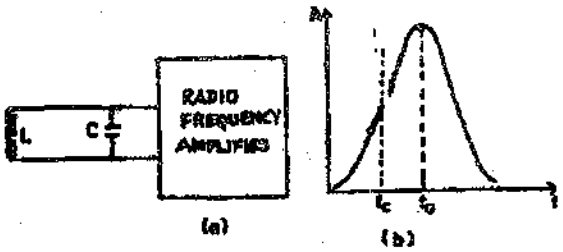

Fig. 22.5 FM detection
(a) Simple FM detector
(b) Frequency Response-Frequency to voltage converter

22.5 SUMMARY

Frequency modulated signal does not consist of noise as amplitude modulated signal.

Modulation index $m_f = \frac{\Delta f}{f_S}$

and f_S is the signal frequency Rf oscillators are used to produce frequency modulated waves.

22.6 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Analyse the expression for a frequency modulated wave.
2. Discuss the principles involved in production and detection of frequency modulated wave.

II Answer the following briefly

1. Derive an expression to represent a frequency modulated wave.

22.7 REFERENCES

1. Electronic Communication Systems	Kennedy Geroge
2. Communication Sys.	Lathi B.P
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4. Electronic Communication Systems	Thomsi
5. Advanced Electronic Communication Sys.	Thomsi Wayne

UNIIT-23: ELEMENTS OF SUPERHETERODYNE RECEIVER

Contents:

23.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of

1) Radio receiver

2) Functioning of a radio receiver

After going through this unit you can discuss the important characteristics of a receiver and explain different electronic units that constitute the super heterodyne receiver.

23.1 INTRODUCTION

Broadcasting stations radiate high frequency radio waves, called the carrier, modulated by the information. A radio receiver should be able to select a desired signal using antenna and a resonant circuit. It is amplified; demodulated and necessary information is recovered. It is then amplified and fed to the speaker, which converts audio signals to sound waves. This complete process is done by a receiver.

23.2 FUNCTIONS OF A RECEIVER

Broadcasting stations radiate high frequency radio waves, called the carrier, modulated by the information (speech or music). The modulator adopted may be AM or FM Regardless of the type of modulation a radio receiver should perform the following functions.

a) Interception of a part of the passing radio waves by the antenna.
b) Selecting the desired signal from the mass of signals intercepted by the antenna. This is achieved by using a LC resonant circuit.
c) Amplification of the received signal before demodulation.
d) Recovery of the information from the modulated wave i.e. demodulation.

e) Strengthening the audio signal recovered from the modulated wave by one or more stages of audio amplification.

f) Conversion of audio signal into sound waves by the loudspeaker.

23.3 AMPLITUDE MODULATED RECEIVER

There are two-types of practical receivers. Tuned radio frequency receiver (TRF) shown in Fig. 23.1 is a simple and straight receiver. It consists of several stages of tuned radio frequency (RF) amplifiers, an AM detector, and one or more stages of audio frequency (AF) amplifiers, driving a loud speaker. In general, a TRF receiver performs well only on a single band, (low frequency or medium frequency). However, it is not practically possible to use this at high frequencies. It cannot discriminate between two by near stations well closer frequencies. This is due to the fact that we are trying to design an RF amplifier to cover the whole broadcast frequency range, which is a difficult task.

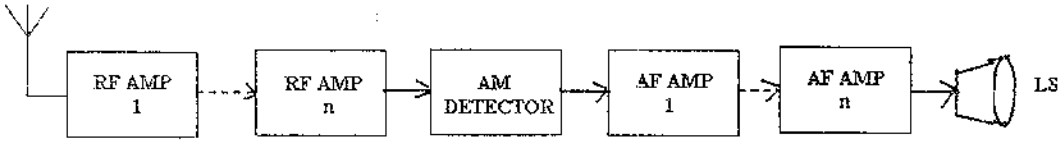

Fig. 23.1 Block Diagram of Tuned Radio Frequency Receiver

23.4 SUPERHETERODYNE RECEIVER

Super heterodyne receiver overcomes this difficulty; it converts all the incoming carrier frequencies into a fixed intermediate frequency (IF). The IF signal is then, amplified by a high gain IF amplifier. It is possible to design highly stable, sensitive and selective amplifiers for a single IF frequency rather than for the whole range of frequencies The IF signal is then demodulated and fed to an AF amplifier and loudspeaker. We shall discuss the working principles of the super heterodyne receiver in this unit. The general block diagram of a simple superheteroyne receiver is shown in Fig. 23.2

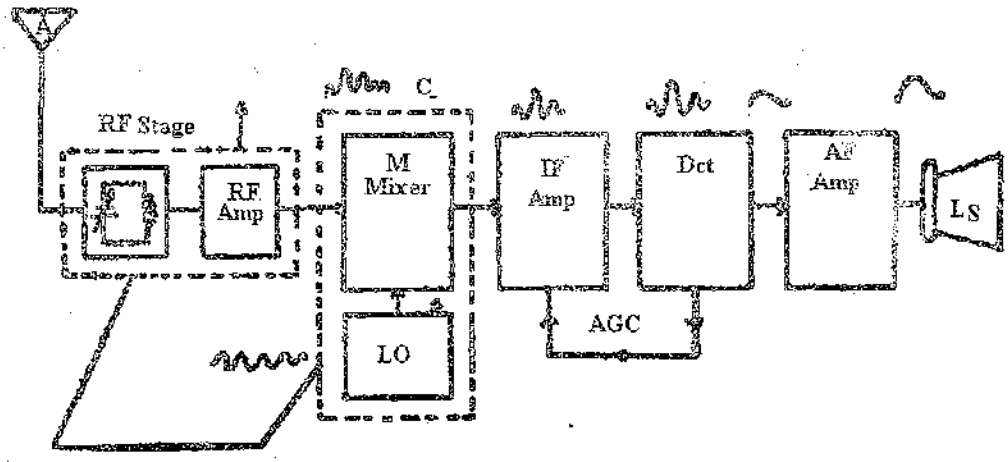

Fig. 23.2 Block diagram of a simple super heterodyne receiver

Antenna (a):

An antenna is a system of electrical conductors, which couples the receiver to space. It intercepts a portion of the electromagnetic energy traveling through space. To effectively intercept energy the antenna should have the proper, size and shape. The dimensions of the antenna should be proportional to the wavelength of the carrier wave i.e., they should be equal to λ or $\lambda/2$ or $\lambda/4$.

Radio Frequency (RF) Stage

The frequency selective tank circuit is tuned to the carrier frequency f_c of the station to be received. It forms the input of RF amplifier. The output circuit of the amplifier is also tuned, to the carrier frequency. The Bandwidth of the RF amplification should be wider enough to accommodate both the sidebands and the carrier. The primary function of RF amplifier stage is to select the desired carrier signal modulated by information and amplify it.

Frequency Converter

The next sage is a frequency converter. It consists of two parts: The frequency mixer and the local oscillator. The mixer, a non-linear device, combines the amplified carrier signal with the output of the local oscillator; the frequency of the local oscillator will be higher than that of the carrier frequency. Local oscillator is tuned such that it always maintains fixed difference in frequency from the carrier frequency. The tuned circuit in the RF amplifier and the local oscillator use capacitors mounted on a common shaft, (they are called ganged capacitors). Once the local oscillator is adjusted to a particular frequency f_O the difference in frequency ($f_O - f_C$) is maintained constant even when tuned to a different station. The output signal from the converter will have fixed intermediate frequency (IF) equal to the difference between the local oscillator and the carrier signal frequencies irrespective of the carrier frequency tuned. It is usually turned to 455 KHz for AM broadcasting. It is to be noted that the IF signal at the output of the converter, though lower in frequency, retains the modulation of the original carrier i.e., it retains the information.

The IF signal is further amplified by the, IF amplifier stages.

Intermediate Frequency (IF) Amplifier:

The IF amplifiers provide the bulk of the receiver gain and thus influence the sensitivity and selectivity of the receiver. The IF amplifier differs from RF stage in the sense that it operates at a fixed frequency. It allows the use of fixed double-tuned inductivily coupled circuits to allow for the sharply defined "Band Pass Response Characteristic" of superheterodyne receivers. It allows accommodating the two side bands along with the carrier. This amplifier works in class-A operation while the mixer stage requires devices to be operated in a non-linear region in order to generate the required difference frequency.

Thus the use of RF amplifier stages increases the signal to appreciable level and makes the mixer, noise of negligible consequence. The bulk of the receiver gain is provided by these IF amplifiers.

Detector (Demodulator)

Next the signal is demodulated in the detector state. Please refer to a detailed explanation

of the working of the detector which is already presented in AM detector. It removes (filters) off the carrier and provides an output containing only the original modulating signals.

Automatic Gain or Automatic Volume Control (AGC OR AVC)

The strength of the signal received from the broadcasting station very often varies due to variations in the space or medium between the transmitter and the receiver. To provide a constant output to the loudspeaker, the radio receiver incorporate an arrangement called automatic gain or automatic volume control. It varies the over all gain of the receiver depending and the strength of the incoming signal. A DC reverse bias voltage, which is proportional to the signal strength, is derived from the detector stage. This bias voltage is used to control the gain of RF, IF and mixer stages. When the incoming signal strength increases the DC detector output voltage also increases this increases in DC detector output. This increases in the DC bias voltage reduces the overall gain of the receiver. In an identical manner decrease in the signal strength decreases the DC reverse bias and hence increases the gain of the receiver and hence increases the output. Thus the receiver output is maintained at a constant level within reasonable limits irrespective of the charges in the amplitude of the incoming signal.

Audio Frequency (AF) amplifier

The audio frequency signals from the detector stage are further amplified by a chain of AF amplifiers until they are sufficiently strong enough to drive a loudspeaker. It is usually one voltage amplifier followed by a power amplifier.

23.5 CHARACTERISTICS OF A RECEIVER

The performance of a receiver is specified by the following characteristics.

a) Sensitivity: It is a measure of the RF signal voltage needed to produce a specified amount of audio power. The overall gain and the noise determine this parameter

b) Selectivity: It is the ability of a receiver to reject unwanted signals. It depends on the sharpness of the resonance curves of the tuned circuits used in RF and IF amplifiers.

c) Fidelity: Indicates how well and truthfully the receiver reproduces the original audio signals. Without introducing distortions in amplitude, frequpon the quality of the AF amplifiers frequency and phase of the original signal. It depends

d) Noise figure: The noise figure determines the smallest power of the signal that may be received without being masked by the noise. It represents one of the most important characteristics of the receivers for the higher frequencies.

Other characteristics, such as power capacity, Harmonic distortion, response to spurious frequencies and cross modulation effects, also are important in deciding the performance of a given receiver.

23.6 SUMMARY

Modulated broadcasting signals are received by a radio receiver with the help of an antenna and resonant circuit. It is amplified demodulated and fed to a speaker. The important characteristics of a receiver are sensitivity, selectivity, and fidelity and noise figure. Dynamic

range and image frequency rejection are also important characteristics of the receiver.

23.7 MODEL EXAMINATION QUESTIONS

I Answer the following question in detail.

1. Give the block diagram of a superheterodyne receiver and explain the function of each block.
2. Give the block diagram of YRF receiver and explain the functioning of each block.

II Answer. the following questions briefly.

1. What is a tuned frequency receiver? What are its disadvantages?
2. Explain the principle of the superheterodyne reception.
3. Define the characteristics of a radio receiver.
4. Discuss the functions of an IF amplifier in a radio receiver.

23.8 REFERENCES

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UNIT -24: TELEVISION TRANSMISSION AND RECEPTION

Contents:

24.0 AIMS AND OB.JECTIVES

This unit explains the principles of
1) TV Transmission and Reception

2) Working of a TV Camera and Receiver

3) Principle of colour T.V. and Functions of different parts of a Receiver

After going through this unit you can discuss

1) The different units of a TV transmitting system
2) Use of a plumbican camera tube.
3) Use of a videcon camera tube
4) Principle of TV Reception and
5) Various stages involved in the TV Reception

24.1 INTRODUCTION

Television is seeing at a distance (tele + vision). In the TV system aural (audio or sound) and visual (video) signals are processed separately. However, the same antenna is used to radiate both the signals. The technique of transmission is similar to that of radio broadcasting.

A TV receiver utilizes the superheterodyne principle like the radio receiver. TV receive.. has to process audio (sound), video (picture) and synchroni ing signals. The basic functions of a TV receiver are

1. Interception of radiated picture and soun sig als. Antenna does this job.
2. Selection of the desired channel signa ror among the different signals intercepted by the antenna.
3. Conversion of RF signal into an intermediate frequency (IF) signal for amplification.
4. Separate detection and amplification of audio and video signals by FM and AM detectors.
5. Separation of sync pulses from the video signal and application of these pulses to generate time base signals. Feeding of these signals to scan coils of the picture tube to reproduce the picture intact.
6. Conversion of audio signal to sound by a loudspeaker and video signal to picture by a picture tube.

24.2 TV TRANSMITTER

The block diagram of a simple TV transmitting system is shown in Fig. 24.1.

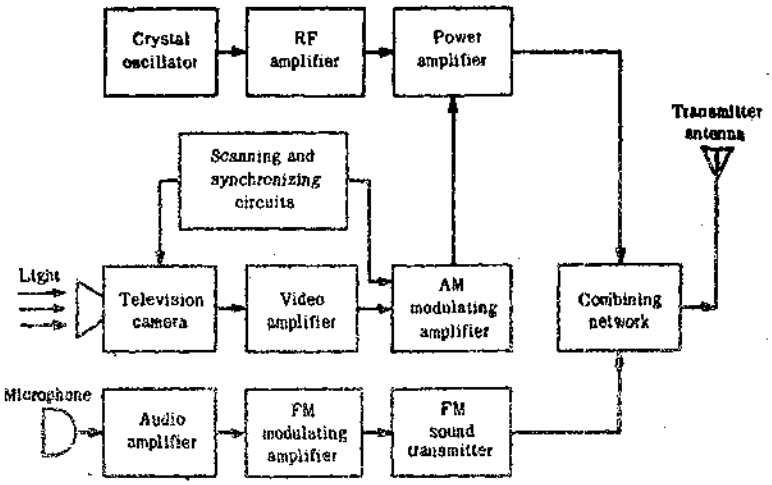

Fig 24.1 Basic block diagram of a monochrome television transmitter

24.2.1 Plumbicon Camera (C)

The camera scans the picture to be transmitted. It converts the original visual information into corresponding electrical signals, namely the Video signals. The amplitude variations of the video signal correspond to the brightness of the picture. The detailed working of camera is discussed latter in this unit.

With a view to see that scanning operations at the transmitter and receiver go in step with each other (i.e. Synchronisation) synchronizing signals are produced at the transmitting station and radiated along with the video signals. These signals are in the shape of rectangular pulses.

They are known as sync pulses. These sync pulses are added to video signal.

24.2.2 Video Amplifier (VA):

This amplifies the composite video signals (Video signals + Sync pulses). The video signals are in the range 10 Hz to 55 MHz. The amplifier designed to amplify the above range of frequencies is called a video amplifier. It is a wide band amplifier that amplifies all frequencies in the range DC to 7.0 megahertz.

24.2.3 Amplitude Modulated Picture Transmitter (AMPT)

This is a circuit, which places visual information on a carrier wave. A radio frequency carrier wave is amplitude modulated by the video signals. The process of amplitude modulation has been discussed in the earlier unit.

24.2.4 Microphone (M)

The microphone converts aural sound information into corresponding electrical signal.

24.2.5 Audio Amplifier (AA)

The signal from the microphone is very weak. It is amplified by using one or two stages of audio amplifiers and then power amplifier.

24.2.6 Frequency Modulated Sound Transmitter (FMST)

The Audio (sound) aural information signal is used to frequency modulate, an rf carrier wave. The carrier used to transmit aural information is 5.5 MHz greater than the carrier frequency used to transmit visual information. Such type of modulating the sound avoids any interference with the picture information. The principles of frequency modulation have been discussed in earlier Unit .

24.2.7 Antenna (A)

A single antenna is used to radiate the AM signal containing visual information and the FM containing aural (sound) information.

24.2.8 Diplexer (D)

To avoid interaction between the two types of signals (i.e.) audio and video and their modulators an electronic switch is used to feed the antenna alternatively with the signals. It is called a diplexer. A diplexer is used for switching between anyone of the two channels A multiplayer is an extension of the same which switches between anyone of the (multi) several channels.

24.3 TV CAMERA AND ITS WORKING

TV camera converts optical image of the picture into electrical image. There are different types of camera tubes. Image orthicon uses the process of photoemission; vidicon, plumbicon and saticon tubes use the process of photoconduction. Plumbicon has several advantages. It is small, light weight, low-power TV camera tube. It has fast response and produces high quality pictures at low light levels. It has a spectral response closest to that of human eye. Hence, the plumbicon tube is widely used, in TV transmission. In view of this we shall confine our study to the plumb icon tube. Fig. 24.2 shows a simplified block diagram of plumbicon tube and the construction of the face plate in Fig.24.2(b)

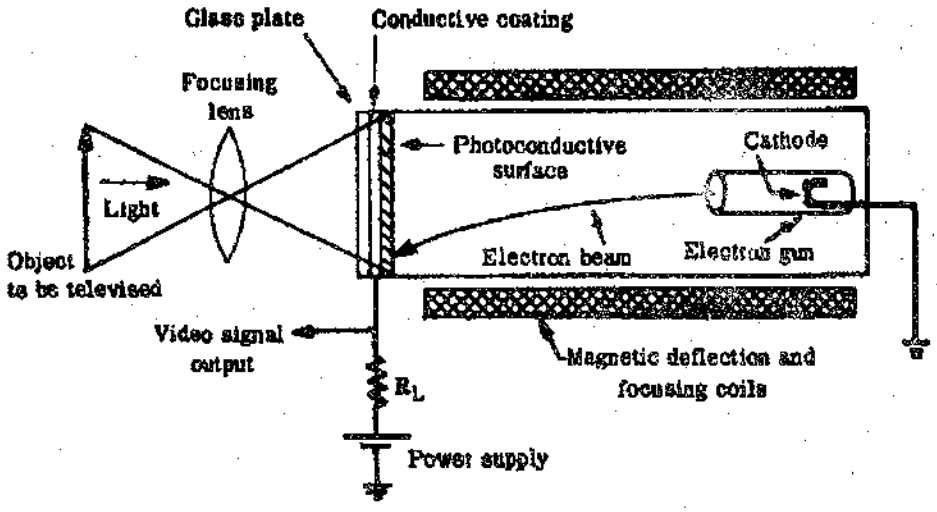

Fig. 24.2 (a)Simplified cross-sectional view of a Plumbicon TV camera tube.

The target is an important element in a video camera. In plumbicon tube it is made up of photoconductive material lead monoxide (PbO). Actually it has three layers. The first one is a thin transparent conductive film of n-type tin oxide (S_nO_2). It is coated on a glass (face) plate. It is also called signal plate of the target. Next to this is a pure photoconductive lead monoxide (PbO) layer, which is an intrinsic semiconductor. The scanning side of lead monoxide has been doped to form a p-type semiconductor (third layer). The lead monoxide layer is granular in structure with individual particles of one-micron size. In the circuit the conductive film of tin oxide (O_2 S_n) is connected to a dc power supply of 4OV through an external resistor R_L. When electron-scanning beam strikes the target it forms a closed loop circuit. The current in the circuit depends on the conductivity of the element where electron beam strikes the target. The conductivity of any target element depends on the brightness of the optical image at that point.

n-type O_2 S_n layer

Glass face plates

I-type PbO

Doped p_type layer

The optical image of the picture to be televised is formed by a high quality zoom lens system. The image is focused through the transparent layer of tin oxide on to the photoconductive lead monoxide. The target is scanned by an electron beam in a particular order (details are explained under scanning). The beam current follows the brightness of the optical image at the point of scan and the load resistor converts the current variations into voltage variations

24.4 SCANNING AND SYNCHRONIZATION

24.4.1 Scanning

The scanning of the target by the electron beam is similar to the way we read a page of print. i.e. from left to right and from top to bottom. In effect the picture is changed into a set of parallel lines called raster. Hence, scanning requires vertical and horizontal deflection systems. The one which moves it steadily from left to right and causes it to 'fly back' rapidly for the scan of next line, is called 'line scan'. The other, the 'field scan' operates simultaneously and moves the beam at a much slower rate in the downward direction (line after line) until the picture is completely scanned and finally it restores back the beam suddenly to the top. Two two pairs of coils mounted round the camera tube form the magnetic deflection system and provide the line and field scans. For high quality picture reproduction, in each complete scan of the target, there should be larger number of scanning lines. The total scan of the target also should occur at a rapid rate. Otherwise the impression of continuity between successive scans is lost and it causes' flicker'. The European TV system has 625 lines and a scan of 50 Hz. In this case the video signal would need a large bandwidth of the order of 8 - 11 MHz. This high value of bandwidth causes circuit design more difficult and it also requires too much of radio wave 'space' so as to prevent overlapping of signals from adjacent channels. This bandwidth requirement can be reduced to half by using" Interlaced' Scanning Technique, in which alternate lines are scanned by election beam producing half picture (312.5 lines) in every 1/50 second and returns to scan the intervening lines (Fig. 24.4). Due to persistence of vision, we will not notice any flicker. All TV systems employ interlaced scanning.

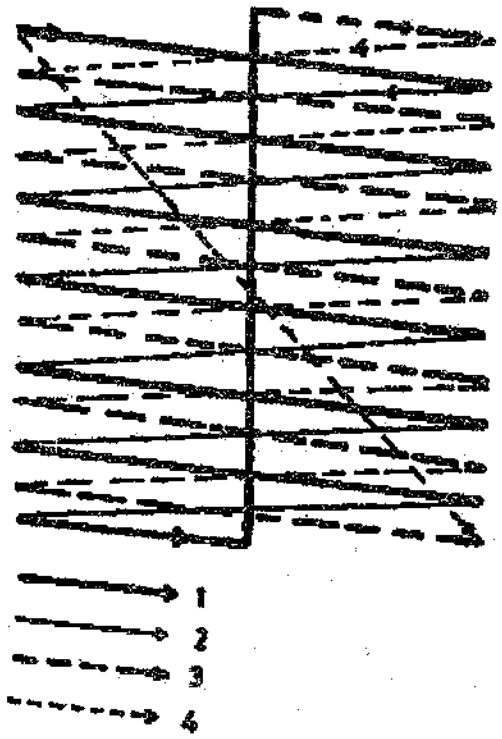

Fig. 24.3 Interlaced scanning
I-First scan_ 2-Fly back of First Scan
3-Second scan; ,4-Fly back of Second Scan

24.4.2. Synchronization

When the TV camera starts scanning line 1 the receiver must also start scanning line 1. When a complete set of horizontal lines has been scanned, moving the electron beam from the end of the bottom line to start the top line (vertical flyback) the retrace must occur simultaneously at both transmitter and receiver. To ensure this, synchronizing pulses are also sent along with picture signal. These are added to the video signal during the fly back times when the beam is blanked out. Thus, the field sync pulses will be longer and less frequent than the line sync pulses. The frequency of field sync pulses will be 50 Hz and the frequency of , line sync pulses will be 50 x 312.5 = 15625 Hz. A simplified wave from with line and field sync pulses is shown in Fig. 23.5.

Fig *24.4* Composite VideO signal
FSP-Field Sync. Pulses
LSP-Line Sync. Pulses
W-White (picture brightness)
B-Black (picture darkest)

24.5 BANDWIDTH REQUIRMENTS

The composite video signal is allowed a 5MHz bandwidth with the highest of video frequency of 5 MHz. The lowest frequency must be the vertical picture scan rate 25 Hz.

This large video bandwidth necessitates the use of VHF-UHF frequencies as RF carrier frequencies. Amplitude modulation of the carrier with the video signal produces two side bands, each 5 MHz wide. This double side band vision signal will occupy a 10 MHz frequency range spectrum with the carrier at the centre. The actual band space allocated to the IV channel will have to be greater still to allow attenuation for an attenuation slope of 0.5 MHz on either side, as the bandwidth cannot abruptly be restricted to 5 MHz.

24.6 PRINCIPLES COLOR TELEVISION

Colour TV uses the fact that any colour may be syntehsized by the addition of three primary colors, blue (B), green (G) and Red (R), in appropriate proportions. For example 100% white light is given by 0.3R + 0.59G + 0.11 B. The principles of transmission are similar to those of the black and white TV. In addition specific colour information must be sent. A practice requirement is that the colour signal must produce a black-and-white picture-on monochrome receiver. In colour TV camera, three plumbicon tubes are required, each viewing picture through a different primary colour filter. The 'red', 'green' and 'blue' signals so obtained provide the required colour information, which is modulated by encoding circuits on a carrir. When added together, they give brightness variations (See Fig_ 24.5).

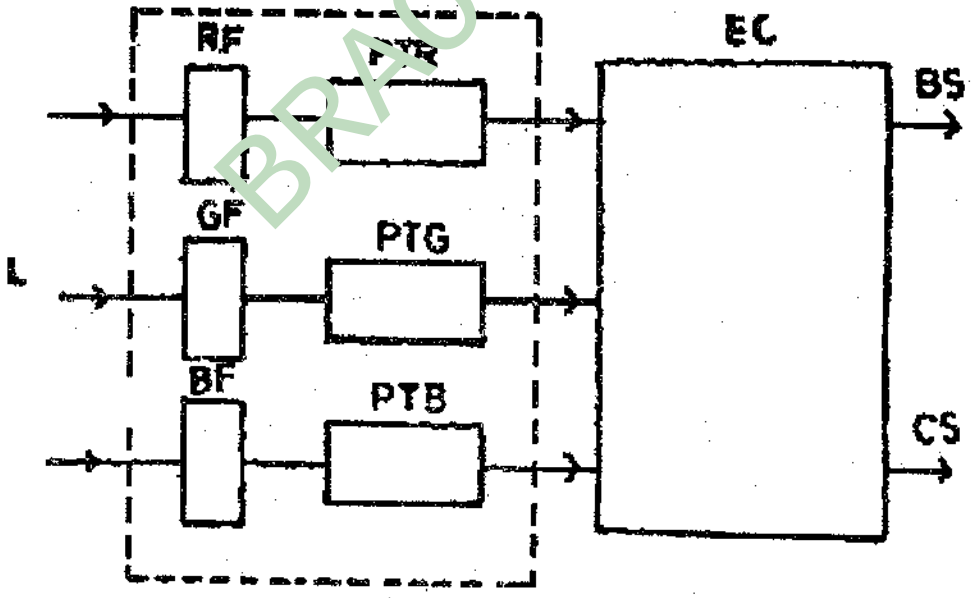

Fig. 24.5 Block diagram of TV receiver

V A-Video Amplifier A-Antenna sc-Scan Coils T –Tuner 'CRPT -cathode Ray picture tube RF A-Radio Frequency Amplifier SS-Sync Separator M-MixerFO-Field Oscillato LIO-Line Oscillator LO-Local Oscillator EHT -Extra High tension Sch-Sound Channel VIP A-Video Intermediate frequency Amplifier VD- Video' detector SIP A-Sound Inter frequency Amplifier SD-Sound detector AFA-Audio Frequency Amplifier LS-Loud Speaker Vch-Video ChaDnel TBCH- Time base channel. AGC-Atuomatic gain control

24.7 TV RECEIVER

The basic elements of a TV receiver for black-and-white monochrome reception are shown in Fig. 24.1.

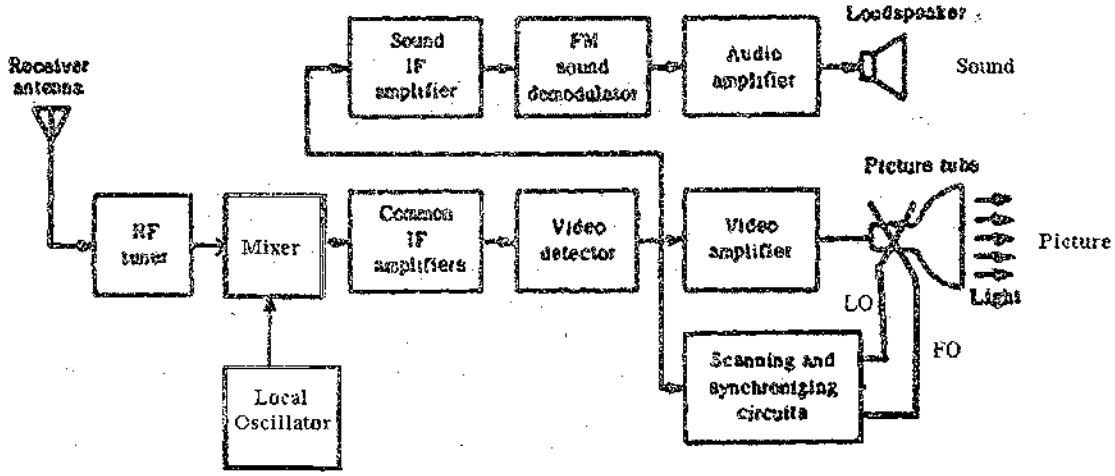

Fig. 24.6 Basic Block Diagram of a Monochrome Television Receiver

Racine Antenna (A)

In a TV receiver the antenna is used to intercept the radio waves carrying video and audio signals transmitted by the television. The position of the antenna must be chosen carefully so *as* to obtain maximum signal strength.

Sometimes signals of the same station, arrive & at the antenna in two or more directions with 4 small time delay. If may be due to the, different paths followed by the signals during their travel. Thus, causes formation of multiple images (usually _called ghost images) on the screen with slight displacement from one another. This can be avoided by using highly directional antenna - that is, an antenna that will receive signals from only one direction. The directional antenna is turned so as to eliminate the undesired signals.

24.7.1 RF Tuner (RF Amp – Mixer – Local Oscillator – Common IF Amp

The front end of the receiver is called the tuner. It consists of the RF amplifier, mixer and local oscillator common IF amplifier stages

1. The RF – Amplifier selects the desired signals and rejects all other and it provides sufficient amplification for strengthens the TV signal.

2. The frequency mixer mixes the RF- signal and local oscillator signal and produces lower beat frequency signal known as Intermediate Frequency (IF) signal as in super heterodyne receiver. It also prevents local oscillator signal from being driven into the antenna and thus radiating unwanted interference signals.

It provides proper impedance matching between antenna and the IF Amp stage.

The TV signal occupies 7 MHz bandwidth in the radio spectrum, arrange far greater than required for a radio reception. So the tuned receiver circuit should have uniform response through out the channel band of 7 MHz and yet selective enough to reject unwanted stations in the adjacent bands. Such circuits are called wide-band tuned circuits. The RF amplifier amplifies the selected signal to a required level the RF signal is converted into IF signal with the help of a mixer (M) and a local oscillator (LO) using the principles of super heterodyne receiver discussed earlier unit. As in radio circuits the gain is controlled by automatic gain control circuits.

24.7.2 Common Video intermediate frequency amplifier (VIF A)

It is also referred to as video IF amplifier even though it is also processing the sound signal, the actual video and sound signals are separated after the common video detector. The sound signal is lather proceeded by another IF stage after it has been extracted from the video detector. The major functions of this stage are given below.

1. It provides most of the radio frequency gain and supplies signals of sufficient amplitude to drive the AM video detector.
2. It provides most of the radio frequency selectively.
3. It reduces accompanying sound interference.
4. It reduces adjacent channel interference.

It has usually two or three stages of video amplifier.

24.7.3 Video detector (VD)

The output of IF amplifier consists of two modulated-IF carrier signals. One is a strong, IF, picture signal. It is rectified using a diode detector and filtered to recover its AM envelope, which is a composite video signal needed for picture tube. The composite video signal contains both picture information and sync pulses.

The other carrier signal contains the frequency modulated sound information. The strong picture carrier beats the relatively weak sound carrier in a non-linear detector stage (heterodyning). Hence, the video detector produces a sound carrier signal at a frequency 5.5 MHz, which is equal to the difference between the sound and video carriers. This is also called inter-carrier sound wave. So the diode detector acts as a second super heterodyne frequency converter for IF sound wave.

24.7.4 Automatic gain control (AGC)

Since the TV receiver, like the radio receiver, may be subjected to widely varying incoming signal strengths some form of automatic gain control is necessary. Both the audio and video signals are stablized by using a negative feedback loop in the receiver. ADC voltage that is decpendent upon the amplitude of sync pulses is extracted and used for controlling the gain of the RF and IF stages.

24.7.5 Video channel (V Ch)

This channel consists of video' amplifiers and 'cathode ray picture tube. The signal amplitude at the output of the video detector is not sufficient enough to drive the picture tube directly. Hence, further amplification is necessary. This is provided by video amplifiers. It

should have uniform response in the frequency range of video signals.

24.7.6 Cathode ray picture tube (CRPT)

It is a part of video section. The picture tube is used to reproduce the picture at the receiver. A monochrome picture tube is a specialized form of the familiar cathode ray tube. It consists of an evacuated bulb containing an electron gun, and fluorescent screen. (Cathode ray tube is discussed in earlier Unit). An electron gun directs a beam of electrons towards a fluorescent material on the screen, which glows when struck by the electrons. Between the gun and screen there are deflection coils (also called scan coils), which deflect the beam horizontally and vertically to form a raster. The brightness of the screen at any point depends upon the number of electrons striking that point. Therefore, the brightness of the picture may be controlled by varying the grid-bias voltage with respect to the cathode voltage. The picture signal from video amplifier, when applied to the grid, changes the instantaneous value of the grid voltage, modulating the intensity of beam current and hence the brightness of the screen. To reproduce the exact picture, the electron beam, which is modulated with picture signal, should scan the screen in exactly the same pattern as in the camera.

24.7.7 Time base channel (TBCh)

It consists of sync separator, field and line oscillators. The composite video signal, which also contains the sync pulses, is processed in the time base channel. The sync separator is a clipper stage that can separate sync pulses from the composite video signal. There are both vertical (at 50 Hz) and horizontal (at 15.625 kHz) sync pulses. The line sync pulses are separated by a high pass filter. They trigger the line oscillator. The field pulses are separated by a low pass filter and they are used to trigger the field oscillator. The oscillators produce sawtooth waveforms, which are further amplified by power amplifiers. The signals are given to the respective scan (deflecting) coils. These time base signals cause the electron beam scan the cathode ray picture tube in exactly the same manner as in the camera and the original picture is reproduced on the screen.

The line oscillator also produces the extra high voltage or tension (E.H.T.) of about 15 to 18 KV required by the final anode of the picture tube. This is essential for a bright picture.

24.7.8 Sound Channel (Sch)

This channel contains IF amplifier detector. AF amplifier and loudspeaker.

The frequency modulated inter carrier sound wave from the video detector is further amplified by sound IF amplifier to a sufficient level. It is demodulated using a FM detector. The detected sound signel is further amplified by AF amplifiers and is fed to a loudspeaker, which converts electrical signals into sound.

24.8 COLOUR TELEVISION RECEIVER

In colour TV, decoding circuits are needed to convert brightness and colour signals back into red, green, and blue signals and special cathode ray tube is required for display.

The common type of display is the DTL tube (Precession in line), which has three electron guns, each producing an electron beam controlled by one of the primary colour signals. Inner

side of the screen is coated with many thousands of tiny lines of red, green and blue phosphors. Between the guns and the screen is the shadow mask consisting of a metal sheet with about half a million slots. As the three electron beams scan the screen under the action of scan coils. the mask ensures that each beam from the respective gun strikes only lines of respective phosphors. Thus we see continuous colour picture.

24.9 SUMMARY

In the TV transmission system Audio and Video signals are transmitted separately by the same antenna. In a TV Camera the most common tube is plumbicon. Mainly T.V. transmitter counts of a Antenna, scanning section and Synchronizing section. A TV receiver consists of antenna, tuner, a cathode ray tube, and video channel, audio channel a time base channel and an automatic gani control system.

24.10 MODEL EXAMINATION QUESTIONS

I Answer the following questions in detail

1 Explain how aural and video signals are processed in a television transmitting system. Give the necessary diagram.
2 Discuss the working of a TV camera.
3 Give the block diagram of a TV receiver and explain its working

II. Answer the following questions briefly

1 What is AGC. How is it achieved?
2 Discuss the need for synchronization in a TV system. How is it achieved?
3 What are the different TV camera tubes in use? Explain.
4 Write a note on the target used in plumb icon tube.

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24.12 GLOSSARY

Modulation	:	The process of changing one of the characteristics of an rf wave according to information.
Detection or Demodulation	:	The process of separating the information from the carrier wave.

Carrier wave	:	A high frequency radio wave which carries information.
Superheterodyne Receiver	:	A radio receiver that converts ail incoming frequency into a fixed intermediate frequency by mixing them with me output of a local oscillator. There after it detects the Information.
Television	:	Seeing at a distance.
Video signal	:	Signals pertaining to the picture to be transmitted.
Side frequency	:	Every modulating frequency gives rise to two frequencies on either side of the carrier wave. They are called side frequencies.

BLOCK – VIII

DIGITAL ELECTRONICS AND MICROPROCESSORS

UNIT - 25: NUBER SYSTEMS, LOGIC GATES AND BOOLEAN ALGEBRA

Contents:

25.0 AIMS AND OBJECTIVES

This unit introduces you to the concept of digital electronics and makes you understand.

1) Decimal & Binary number system and

2) Binary Algebra

3) The Basic Boolean Operators like AND OR NOT

4) De Morgan's Theorem and

5) Logic Gates that Perform Boolean Operations.

After going through this unit you will be able to interconvert

1) One number system into another and vice versa

2) Add, subtract different numbers

3) The working of electronic circuits, which can perform Boolean operations between two logic levels 1 and 0.

25.1 INTRODUCTION

We are very familier with decimal number 0 to 9. There are several other number systems like binary, octal and hexa decimal etc. which are more suitable to be used by the microprocessors. They are the heart of any digital computer. To work with the numbers systems separate algebra was devolped by Geroge Boole. Several arithmetic and logical circuits were also designed for carrying out these Boolean operations

25.2 NUMBER SYSTEMS AND INTER CONVERSIONS

1. Binary Numbers:

A number system is a code representing quantities. Each quantity is represented by a symbol. In the familiar decimal system we use ten digits (0 to 9). When the count exceeds 9, we place 1 in a second position to the left of the units position to represent tens. A third position to the left of the tens position gives hundreds and. so on. The values of the successive positions starting from right one 1, 10, 10 etc. or in powers of ten 10^0, 10^1, 10^2, etc.

For example the number twelve hundred thirty four is written in decimal system as.

$$1234 = (1 \times 10^3) + (2 \times 10^2) + (3 \times 10^1) + (4 \times 10^0)$$

In other words, 10 is the base and each position to the left corresponds to an increasing power of ten. In the binary number system the base is two. We use only two digits 0 and 1. The digits 0 and 1 are called bits (binary digits). Successive positions in this system represent, from the right, powers of 2 i.e. 2^0, 2^1, 2^2, 2^3 etc. This system is convenient for counting in electronic systems. This is because of the fact that an electronic device has two states ON or OFF. Its output is high or Low representing 1 or O. High and Low values of the output correspond to certain conventionally accepted voltages specified by the circuit designer. For example in a particular system zero corresponds to a voltage near zero and 1 corresponds to + 5V.

The decimal number 10 in the binary system can be written as

$1010 = 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$= 8 + 0 + 2 + 0 = 10$ (decimal)

25.2.1 Binary-to-Decimal Conversion:

To convert a binary number to its decimal equivalent, add the decimal equivalents of each position occupied by al.

For example

$$110001 = 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$$
$$= 32 + 16 + 1 = 49$$

$$101.0101 = 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}$$
$$= 4 + 0 + 1 + 0 + \tfrac{1}{4} + 0 + 1/16 = 0 + 0.25 + 0 + 0.0625 = 5.3125$$

25.2.2 Decimal-to-Binary Conversion

To convert a decimal integer to its binary equivalent, progressively divide the decimal number by 2, noting the remainders. The remainders taken in reverse order are the binary equivalent. This is called the double-dabble method.

The decimal numbers are:

30.375	and	25.85
30 ÷ 2 = 15 with a remainder 0		25 ÷ 2=12 with remainder 1
15 ÷ 2 = 7 with a remainder 1		12 ÷ 2=6 with remainder 0
7 ÷ 2 = 3 with a remainder 1		6 ÷ 2=3 with remainder 0
3 ÷ 2 = 1 with a remainder 1		3 ÷ 2=1 with remainder 1
1 ÷ 2 = 0 with a remainder 1		1 ÷ 2 with remainder 1
Hence the binary equivalent of 30 is 11110		The Binary Equivalent of 25 is 11001

(c) To convert a Decimal Fraction to its binary equivalent: Progressively multiply the fraction by 2, removing and noting the carrier, the carrier taken in the forward order with the decimal is the binary equivalent.

For example

0.375 x 2 = 0.75 with a carry of 0	0.85 x 2 = 1.7 = 0.7 with carry of 1
0.75 x 2 = 1.50 with a carry of 1	0.7 x 2 = 1.4 = 0.4 with carry of 1
0.50 x 2 = 1.00 with a carry of 1	0.4 x 2 = 0.8 = 0.8 with carry of 0
	0.8 x 2 = 1.6 = 0.6 with carry of 1
	0.6 x 2 = 1.2 = 0.2 with carry of 1
	0.2 x 2 = 0.4 = 0.4 with carry of 0
The binary equivalent of 0.375 is .011	The binary equivalent of .85 is 0.110110
Hence, (b + c) the binary equivalent of 30.375 is 11110.011.	Hence, (b + c) the binary equivalent of 25.85 is 11001.110110.

25.3 BINARY ADDITION AND SUBTRACTION

Binary arithmetic is similar to that of the decimal one. In binary addition, we add position by position carrying where necessary to higher position. Binary addition is easy as we have to deal with only four cases.

0+0=0
0+1=1
1+0=1
1+1=10

and

In the fourth case, 1 plus 1 equals 002 in decimals system which in binary is 10. The right position is 0 and 1 is carried to the next position column on the left.

Let us now add the following binary number

```
  11
 +11
------
 110
------
```

The answer is obtained as follows: In the last significant (right hand) column

1 + 1 = Sum 0 + Carry 1

In the next column three bits have to be added, Le.

1 + 1 + 1 = Sum 1 + Carry 1

25.3.1 Direct Subtraction:

In subtraction we subtract column by column borrowing from higher position columns, wherever necessary. The binary subtraction is also easy as we have to deal with only the following four cases:

0-0=0
1-0=1
1-1=0
10-1=0

Example -I

```
1101      =     13
-1010     =    -10
--------        ---------
0011      =     +03
--------        ---------
```

25.3.2 Subtraction Through 1's compliments:

To facilitate subtraction by electronic circuitry a new process has been evolved. It is called the one's complement method. In order to subtract 1010 from 1101 we proceed as follows:

(a) Form one's complement of 1010: this is done by changing 1's to 0's and 0's to 1's. Thus the ones complement of 1010 is 0101

(b) Add the one's complement from (a) to the number from which subtraction is to be made i.e. add 0101 to 1101

```
  1101
+ 0101 (1's compliment of 1010)
  1010
```

(c) If there is a carry in the most significant position of the total in (b), remove it and add the same to the remaining four bits to get the answer that is

```
10010  0010
     + 0001
     ------
      0011   =   3
     ------
```

The carry that is added is called the end-around carry or EAC. if there is an EAC, the answer is positive. If there is no carry, the answer is negative.

Example – II

10	1010
-13	+0010
-----	--------
-03	1100

Taking the one's complement of 1100 we get the answer as 0011 (3) since there is no EAC, the answer is negative.

Binary multiplication and division can be performed by repeated addition and subtraction respectively.

25.4 BINARY-CODED-DECIMAL

For convenience the results of a binary operation is very often displayed in the decimal form. BCD is a variation of the binary code. It facilitates easy conversion of binary numbers into decimal numbers. In this code, each digit of a decimal number is expressed in terms of its binary equivalent instead of the whole number. This will be comber some for numbers large number of bites

For example,
Decimal

3 8

is 0011 1000 in BCD

However, the actual binary equivalent of

38 is 1001100

similarity the following numbers are BCD expressed in BCD as shown below

4 5 . 3 6

0100 0101 . 0011 0110

7 3 6
0111 0011 0110

6 9 7 6 . 8 5 4
0110 1001 0111 0110 1000 0101 0100

The actual binary equivalents of the last decimal numbers becomes so much un necessary large and hence BCD conversions are adopted and all the modern computers are designed to accepts these BCD numbers directly

25.5 OCTAL NUMBER SYSTEM

25.5.1 Octal Numbers:

This unit introduces you to the concept of octal numbers, which are important in digital work as certain digital systems and Microprocessors work on octal number system. The digits in an octal system are

0, 1, 2, 3, 4, 5, 6, 7

These digits 0, 1, 2, 3....., 7 have the same physical meaning as the decimal symbols. In order to count numbers greater than 7, two-digit combinations (that as in decimal system) is used. After exhausting the 2 digit combination, 3 digit combination, 4 digit ..... and higher digit combinations are used to represent higher numbers.

0, 1, 2, 3, 4, 5, 6, 7
10, 11, 12, 13, 14, 15, 16, 17,
20, 21
30,
40,
50,
60,
70, 71, ..., 77
100
110

The octal numbers have a base of 8

Representation of an octal number

etc.,<-- $DX8^3 + CX8^2 + BX8^1 + AX8^0 \bullet aX8^{-1} + bX8^{-2} + CX8^{-3} + dX8^{-4}$ →etc.,

Octal point

25.5.2 Conversion of Octal number into Decimal Number

The octal number 257 is represented as 257_8 and can be converted decimal number as

$2 \times 8^2 + 5 \times 8^1 + 7 \times 8^0 =$

$2 \times 64 + 5 \times 8 + 7 \times 1 = 128 + 40 + 7 = 175|_{10}$

25.5.3 Conversion of Decimal Number into Octal Number

The Octal number is to divide the number by 8 just as we divide by 2 in binary conversion. Converting $175|_{10}$ to octal

```
8 | 175        Remainder
8 | 21  ---->    7   ^
8 |  2  ---->    5   |        i.e., 257|8
     0  ---->    2   |
```

25.5.4 Conversion of decimal fractions into octal fractions

we multiply successively by 8 just as we multiplied by 2 in binary conversion. Converting 0.23_{10} to octal

```
0.23X8 = 1.84 = 0.84    with a Cary    1 |
0.84X8 = 6.73 = 0.72                   6 |
0.72X8 = 5.76 = 0.76                   5 v
etc.,
```

$0.23|_{10} = 0.165|_8$

25.5.5 Conversion of Octal fraction to Decimal fraction

Multiplying by the positional weightages we can convert the octal fraction to decimal fraction as

$0.165_8 = 0.1X8^{-1} + 6X8^{-2} + 5X8^{-3}$

$= 0.125 + 0.09375 + 0.009765625 + \ldots$

$= 0.228\ldots|_{10}$

25.5.6 Conversion of Octal number to Binary and Binary to Octal

To convert an octal number into its binary equivalent, convert $23|_8$ into binary equivalent

2	3	
010	011	i.e., $23_8 = 010\ 011$

Conversion of binary number into its equivalent octal number as $3547|_8$

3	5	7	4	
011	101	111	100	i.e., $3574|_8 = 011\ 101\ 111\ 100$

To convert mixed binary numbers into octal numbers separate the binary numbers into groups of 3 digits and give the appropriate octal value to it.

1011 . 01101

001	011 .	011	010
1	3	3	2

i.e., $1011.01101|_2 = 13.32|_8$

25.6 HEXA – DECIMAL NUMBERS

All the modern digital computers make use of Hexadecimal numbers for their operation. The Hexadecimal is simply denoted as Hex has a base of 16. The digits in the Hex system are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F. In order to count any number higher than 16, the 2 digit, 3 digit ….. etc. and higher digit combinations are used.

0, 1, 2, ... 9, A, B, ...F
10, 11, 12, ...19, 1A, 1B, ...1F
20, 21, 22, ...29, 2A, 2B, ...2F
30, 31, 32, ...39, 3A, 3B, ...3F etc.,
.
.
.
90,91,92,.....99,9A,9B,.....9F etc.

25.6.1 Conversion of Hexadecimal number into its Binary equivalent

To convert any Hex number like $B27A3|_H$ into its binary equivalent give the binary weightage to each digit as shown below

B27A3 ------ B 2 7 A 3.

1011 0010 0111 1010 0011

$B27A3|_H = 1011\ 0010\ 0111\ 1010\ 0011|_2$

In order to convert a binary number into its Hexadecimal number, separate the binary digits into groups of 4 digits and give the appropriate Hexadecimal value to it as.

To convert $10011101|_2$ = 1001 1101
9 D

$1001\ 1101|_2 = 9D|_H$

25.7 BOOLEAN ALGEBRA

George Boole, an English mathematician formulated the rules governing the algebra of the binary system; hence the name. Boolean algebra is a valuable tool in manipulating binary variables and operators (OR, AND, NOT etc.).

Boolean expressions contain only two variables i.e. 0 and 1. The result of a Boolean operation can only be 0 or 1. The basic Boolean operators are;

AND a single dot between the variables

$\overline{A \bullet B}$ – A and B

OR

a + between the variables

$\overline{A+B}$ - A or B

NOT (or Negation or Inversion) a - (bar) over the variable

$\bar{A}$ ———— not A. It represents the complement of A.

The basic postulates of the binary algebra are presented in the truth tables given below.

Operator	OR	AND	NOT
Postulate	A +B = Y	A .B = Y	A=Y
	0 + 0 = 0	0.0 = 0	$\bar{0} = 1$
	0 + 1 = 1	1.0 = 0	$\bar{1} = 0$
	1 + 0 = 1	0.1 = 0	---
	1 + 1 = 1	1.1 = 1	---

Just as in ordinary algebra we have commutative, associative and distributive rules in Boolean algebra. They are

Commutative: A+B=B+A
A.B = B.A

Associative: A+B+C = A + (B +C) = (A+B)+C
A.B.C = A. (B.C) = (A.B)C

Distributive: A. (B+C) = A.B + A.C
A + (B.C) = (A + B)C

In addition we have two powerful theorms called De Morgan's theoroms. They are

$$\overline{A+B} = \bar{A} \bullet \bar{B}$$
$$\overline{A \bullet B} = \bar{A} + \bar{B}$$

25.8 PROOF OF DE MORGAN'S THEOREMS

Theorem 1: The complement of the sum of two variables is equal to the product of the complements. Proof:

$$\overline{A+B} = \bar{A} \cdot \bar{B} \qquad \ldots(25.1)$$

i. A= 0, B=O
$\overline{A+B} = \overline{0+0} = 0 = 1$
A.B=0.0=1.1=1

ii. A = 0, B = I
$\overline{A+B} = \overline{0+1} = \bar{1} = 0$
$\bar{A} \cdot \bar{B} = 0.1 = 1.0 = 0$

iii. A = 1, B = 0
$\overline{A+B} = \overline{1+0} = \bar{1} = 0$
$\bar{A} \cdot \bar{B} = 0.1 = 0$

iv. A=1,B=1 $\overline{A+B} = \overline{1+1} = \overline{1} = 0$

$\overline{A} \cdot \overline{B} = \overline{1} \cdot \overline{1} = 0.0 = 0$

Hence for all combinations of A and B, the relation (25.1) is proved to be valid. That is complement of the sum of two variables is equal to the product of their complements.

$$\overline{A+B} = \overline{A} \cdot \overline{B} \qquad \ldots(25.2)$$

Theorem 2: The complement of the product is equal to the sum of the complements.

$$A \cdot B = \overline{A} + \overline{B}$$

Proof:

i. A = 0, B = 0 $\overline{A} \cdot \overline{B} = \overline{0}.\overline{0} = \overline{0} = 1$

$\overline{A} + \overline{B} = \overline{0} + \overline{0} = 1 + 1 = 1$

ii. A = 0, B = 1 $\overline{A} \cdot \overline{B} = \overline{0}.\overline{1} = \overline{0} = 1$

$\overline{A} + \overline{B} = \overline{0} + \overline{1} = 1 + 0 = 1$

iii. A = 1, B = 0 $\overline{A} \cdot \overline{B} = \overline{1}.\overline{0} = \overline{0} = 1$

$\overline{A} + \overline{B} = \overline{1} + \overline{0} = 0 + 1 = 1$

iv. A = 1, B = 1 $\overline{A} \cdot \overline{B} = \overline{1}.\overline{1} = \overline{1} = 0$

$\overline{A} + \overline{B} = \overline{1} + \overline{1} = 0 + 0 = 0$

Hence for all combinations of A and B the selection (25.2) is proved to be valid. That is the complement of product of two variables is equal to the sum of their compliments.

$$\overline{A.B} = \overline{A} + \overline{B}$$

25.9 LOGIC GATES

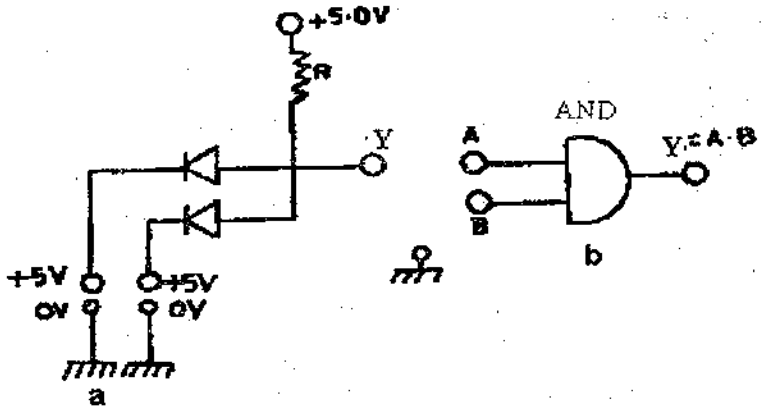
Logic gates are electronic circuits that perform Boolean operations. They are electronic circuits that control the flow of information in the form of pulses. Their inputs and outputs have only two levels of voltage, called' High' and 'Low'. High level is closer to the supply voltage (ex: + 5 Y for a particular type of IC gates) and Low level is closer to OY (+ 0.8Y and less). High is referred to as logic level 1 and low is referred to as logic level 0.

Logic gates may be realized using diodes and resistor or transistors and resistors. Each gate is represented by a symbol. Its behavior is indicated by its Truth Table. It shows the output of the gate for all possible combinations of inputs. Let us now discuss the working of the basic gates.

AND Gate:

A simple circuit to illustrate the working of the gate is shown in Fig. 25.1 along with its symbol and Truth Table.

Fig. 25.1(a) shows a two-input AND gate. Here A and B are the inputs and C is the output. For the moment, let us analysis this AND gate by restricting the input voltages to either 0 or 1. There are only four possible cases to analyses



A	B	Y=A .B
0	0	0
0	1	0
1	0	0
1	1	1

C

Fig. 25.1 Two-input NAND gate
(a) Circuit (b) Symbol(c) Troth table

Case 1: A=0 and B=0. Since both the inputs are at OV they are like short. The 1V means 5V (in the fig) battery force conventional current in the direction of each diode there fore both diodes are on or shorted. Hence the output is shorted to ground through the diodes there fore Y=0

Case 2: A=0 and B=1. The upper diode in forward biased the output is shorted to ground through the upper diode. The force Y=0.

Case 3: A=1 and B=0 This also similar to case 2, and hence Y = 0.

Case4: A=1and B=1. No current flows in the circuits. Whe there in no current in R, there is no voltage drop across R; there fore, Y in equal to 1V.

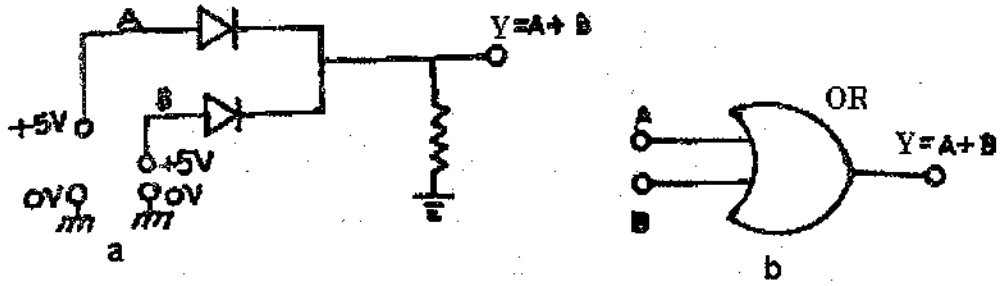
Remember that "output is 1 only when all inputs are 1's ."

OR Gate:

The circuit diagram of a simple diode-resistor OR gate. its symbol, and the truth table are shown in Fig. 25.2.

Consider again the two-input OR gate. Fig (25.2). Again use ideal diodes and restrict all voltages to either 1 or 0these are only four possible cases to analyze.

Case 1: A=0 and B=0 with both the input voltage at zero, he out put voltage also zero, because there exists no voltage any where in the circuit. There force Y=0.



C →

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 25.4 Diode OR gate
(a) Circuit (b) Symbol (c) Truth table

Case 2: A=0 and B=1 The 'B' input forward bias as the lower diode, causing the output 1V. Since the input A in O V, it looks like a short. There fore the upper diode is off and the lower diode is on over hence the output Y=1 V

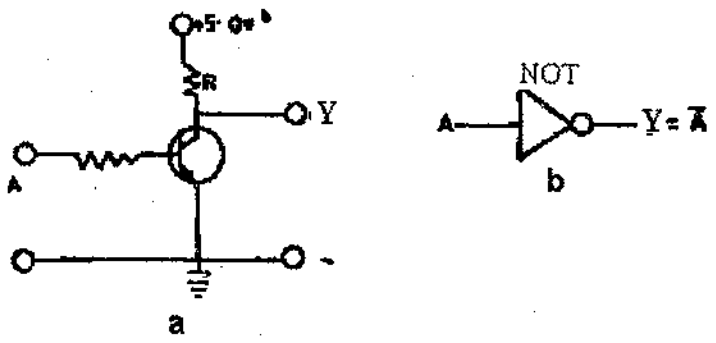
Case 3: A=1 and B=0. the arrangement in similar to case 2, Here the upper diode is on, the lower diode is off and hence the output Y=1 V.

Case 4: A=1 and B=1 . When both the inputs are at 1V , both the diodes are forward biased. Since the voltages are in parallel the output voltage is 1 V. there fore Y=1 V.

After the discussion at the end incorporate. Remember, **"Output is one if any one of the inputs is one and output is zero when all the inputs are zero".**

NOT Circuit:

A single stage transistor amplifier inverts the input signal, hence it acts as a NOT gate.The circuit diagram, symbol and the truth table of the gate are shown in Fig. 25.3.



A	Y
1	0
0	1

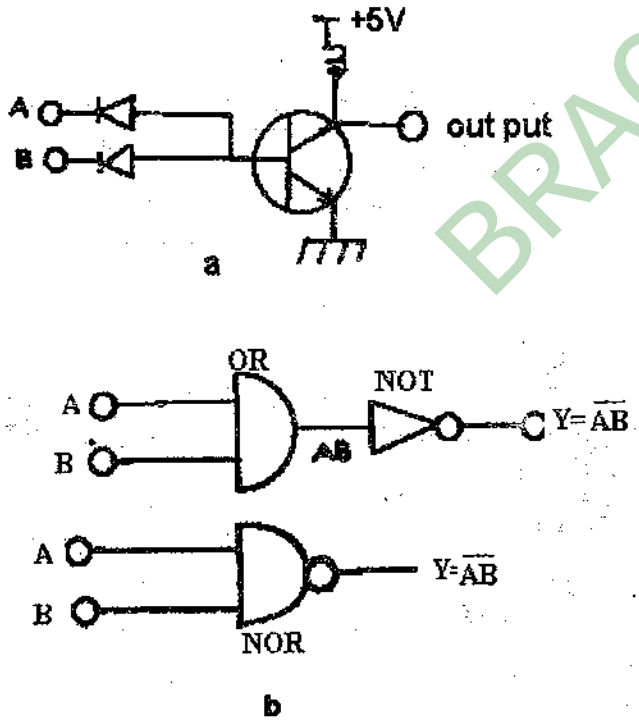
(c)

Fig. 25.3 Not Gate (a) Circuit diagram (b) Symbol(c) Truth table

It has one input terminal and one output terminal. It produces a' High output or 1 when the input is Low or 0. Similarly it produces a low output or 0 when the input is High or 1. It is called NOT circuit because its output is 'High' if the input is NOT High. Whatever is the input, this gate' inverts' it or compliments it.

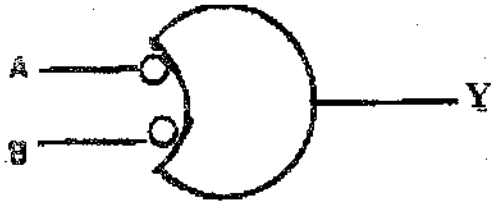
NAND gate:

This is a combination of AND and NOT gates (NOT AND = NAND). The truth table can be worked out using the truth tables of the NOT and AND gates. It is shown in the figure. As is evident from the truth table, its characteristic can be summed up as



A	B	Y=A.B
0	0	1
0	1	1
1	0	1
1	1	0

(c)



(d) Bubbled OR

A	B	Y=A.B
0	0	1
0	1	1
1	0	1
1	1	0

(e)

Fig.25.4 NAND Gate
(a) circuit (b) Symbol (c) NAND Truth table
(d) Bubbled OR gate (e) Bubble Truth table

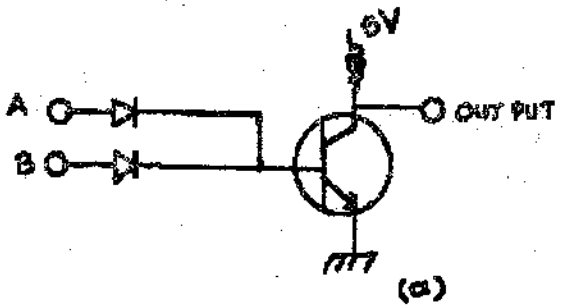
"Out put is one if any one of the input is zero, and output is zero when all the inputs are one."

Bubbled OR Gate:

The truth table of the bubbled OR Gate is shown in fig (25.4) this truth is identical to that of the NAND gate. Hence it is possible to replace the NAND gates with bubbled OR Gate or Vice-versa

NOR Gate:

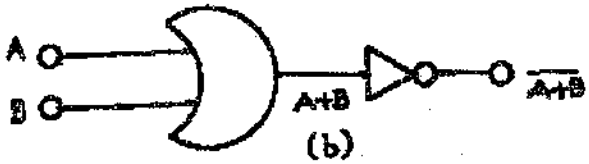
A NOT-OR gate with two inputs simulates the NOR function. The circuit, symbol, and the truth table of this gate are given in Fig. 25.5. If either or both A and B are High, the transistor conducts and the output is 'LOW'. When both the inputs are 'LOW' i.e. neither A NOR B is 'High', the output is high. A NOR gate can be also represented as OR gate followed by an inverter (NOR) though only two input gates are discussed in this unit gates with more than 2 inputs are also used in digital circuits



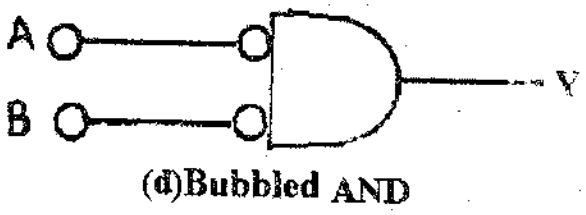
(a)

A	B	$Y = \overline{A} \bullet \overline{B}$
0	0	1
0	1	0
1	0	0
1	1	0

(c)



(b)



(d)Bubbled AND

A	B	$Y = \overline{A} \bullet \overline{B}$
0	0	1
0	1	0
1	0	0
1	1	0

(e)

Fig. 25.5 NOR gate (a) Circuit (b) Symbol (c) NOR Truth Table

(d) Bubbled AND gate (e) Bubbled Truth table

Bubbled AND Gate:

The truth table of the bubbled AND Gate is shown in fig (25.5) this truth is identical to that of the NOR gate. Hence it is possible to replace the NOR gates with bubbled AND gates.

25.10 SUMMARY

Binary numbers can be converted into decimal numbers and vice versa. Binary numbers can be added and subtracted using the principles of binary Algebra.

Boolean expressions contain only two variable 0 and 1. Electron circuits are used to perform logic operations involved in Boolean algebra.

25.11 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Explain the working of the following logic gates using simple circuits: AND, NOT and OR.
2. Give the truth tables of the following gates OR, AND, NOT, NAND and NOR.

II. Answer the following questions briefly.

1. What are logic gates? What is their use? What is a Truth Table?
2. Explain bow you would convert a binary numbers to the decimal equivalent.
3. Explain bow you would convert a decimal numbers into its binary equivalent.
4. Explain bow you would convert a decimal number into binary equivalent
5. Explain bow you would add and subtract two binary numbers.

25.12 REFERENCES

1. Pulse and digital electronics — Jacob Millman and Taub Herbert
2. Digital Integrated Electronics — Taub Herbert and Schilling
3. Digital Design — Moris Mano
4. Digital principles and applications — Malvino.A.P. and Leach.D.P.
5. Pulse and Digital Electronics — Mithal..G.K.
   Digital Electronics by RP Jain

UNIT - 26: COMBINATIONAL LOGIC CIRCUITS: HALF ADDER AND FULL ADDER

Contents:

26. 0 AIMS AND OBJECTIVES

This unit gives an idea of

1. Exclusive OR gate
2. Half adder and Full adder

After going through this unit you will be in a position to explain

1. The Working XOR gate
2. Add two or three bits at a time.

26.1 INTRODUCTION

The exclusive OR gate has two inputs and one output. The output is a 1 when either of the inputs is at 1 but' 0' when both inputs are same. Half adder and Full Adder adds simultaneously two bits and three bits respectively.

26.2 EXCLUSIVE OR GATE (XOR)

We have studied the Truth table of the OR gate in the previous lesson. The output of the OR gate is 1 if either of its inputs is 1. It gives a 1 output even if both inputs are 1. This is not suitable to binary addition. We would like to have a gate which gives a 1 output only when either of its inputs is 1. It should not give 1 output when both inputs are 1. The Exclusive OR gate satisfies this requirement. Its equivalents symbolic representation is shown below

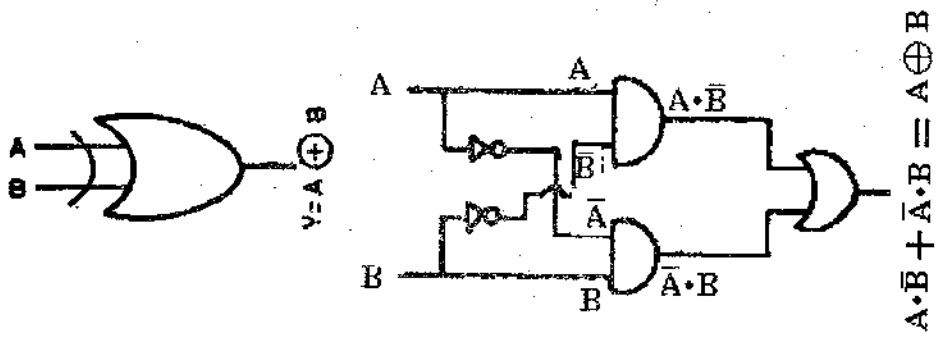


Fig.26.1 X-OR gate

The truth table for this gate is shown in Table 26.1

Table 26.1 Truth table for XOR

INPUTS		Output
A	B	Y=A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

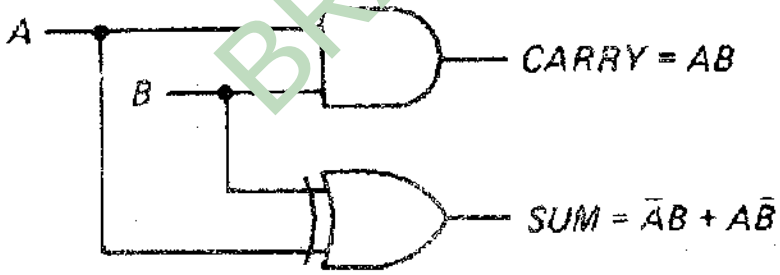
It can be seen from the above that its output is 1 when A = 0 and B = 1 and when A = 1 and B = O. This can be expressed in algebraic form as

$$A \oplus B = \overline{A}B + A\overline{B}$$

The XOR can be constructed using the basic gates discussed in the previous Units.

26.3 HALF-ADDER

Let us now consider the "process of binary addition. When we add two binary numbers the sum of 0 or 1 and a carry of 0 or 1 result. An examination of the truth table for XOR shows that it is ideally suited for this purpose. It gives the sum of any two binary numbers. We have to make an arrangement to get carry of 1, when we add 1 and 1. This can be done by using an AND gate and XOR gate as shown in Fig. 26.2,



. Fig. 26.2 Half adder

Both the inputs are given simultaneously to the XOR and AND gates. The Output of the XOR gives, as explained in the last section, the sum of the two binary inputs for all the possible combination of inputs. If A = I and B = 1 we need a carry 1 which is obtained at the output of the AND gate. The truth table for the half adder is shown in Table 26.2

Table 26.2 Truth table for the Half-Adder

A	B	Sum S	Carry C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The half-adder can add only two single digit numbers. We cannot add three or multi-digit numbers using the half-adder. Hence it is called the half-adder.

Two half-adders and an OR gate can be used to add three digits.

26.4 FULL-ADDER

It consists of two half-adders and an OR gate. It has three inputs and two outputs. It can accept two digits and a carry signal from the adjacent column. The circuit diagram of the full adder is shown in Fig. 26.3

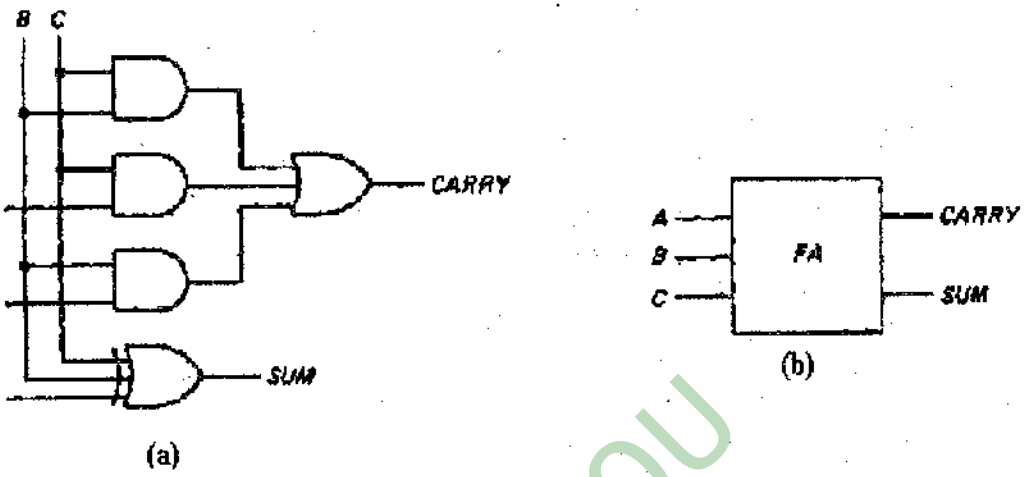


Fig. 26.3 (a) Full-adder (b) Symbol

Let us now examine how the full-adder performs addition of three digits. Let A = 1, B = 0, and C = 1. The Half-adder-1 gives sum of 1 and a carry 0. The half-adder -2 has 1 and 1 as its inputs. This leads to a sum 0 and carry 1. As a consequence the inputs to the OR gate are 0 and 1. This leads to a carry 1 and sum 0 at the output of the full-adder. In this way we may work the Truth Table for full-adder which is shown in Table 26.3.

Table 26.3 Truth Table for the Full-Adder

A	B	C	S	C
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
0	0	1	1	1
1	1	0	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

To perform the addition of 4-bit words I we need a half-adder for the first column and a full adder for each additional column. The input to the half-adder consists of digits A_1 and B_1, for the first column. The input to the next unit, a full adder, consists of carry C_1 from the first column and digits A_2 and B_2 for the second column. This is called parallel binary adder. It is shown in Fig. 26.4.

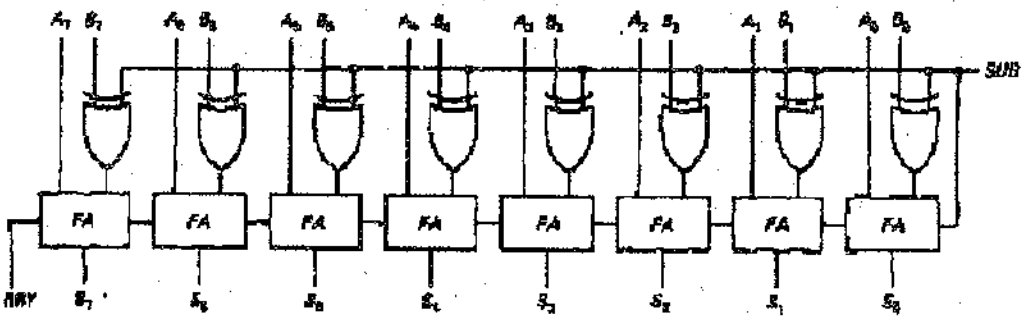


Fig. 26.4 Parallel binary adder.

26.5 SUMMARY

The behavior of XOR gate is slightly different from that of ordinary OR gate Combinational logic circuits like half adder and full adders are used for binary addition.

26.6 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail.

1. Explain the working of half and full adders.

II. Answer the following questions briefly.

1. Explain the working of the XOR gate.
2. Discuss the working of a half adder.
3. Discuss the working of a Full-adder.

26.7 REFERENCES

1.	Pulse and digital electronics	Jacob Millman and Taub Herbert
2.	Digital Integrated Electronics	Taub Herbert and Schilling
3.	Digital Design	Moris Mano
4.	Digital principles and applications	Malvino.A.P. and Leach.D.P.
5.	Pulse and Digital Electronics	Mithal..G.K.
6.	Digital Electronics	RP Jain

UNIT- 27: SEQUENTIAL LOGIC CIRCUITS: FLIP-FLOPS AND COUNTERS

Contents:

27.0 AIMS AND OBJECTIVES

This unit explains you the concept of

1) Flip Flops

2) Different types of Flip Flops and

3) Binary and Decade Counters

After studying this unit you will be able to explain

1) The operation of RS, RST and JK Flip Flops

2) The working of binary counter

27.1 INTRODUCTION

Flip Flops or Multi vibrators are switching circuits with two stable states. The output of these circuits depends not only on the present input but also on the previous inputs as well. Hence Flip Flops may be realized using NAND gates. The important property known as toggling of the Flip Flop is utilized in the construction of binary and decade counters and memory units.

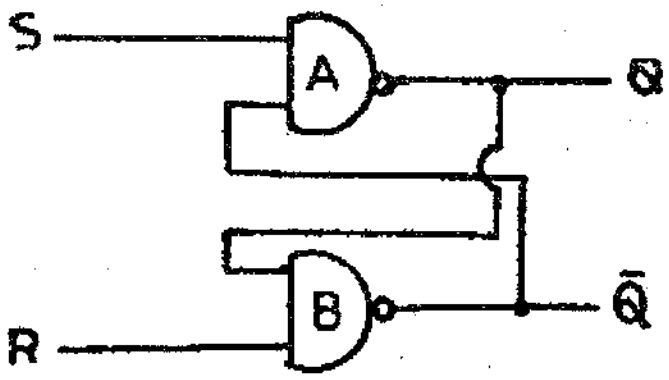
27.2 RS FLIP-FLOP

The $\overline{RS}$ Flip Flop consists of two NAND gates connected as shown in Fig, 27.1

The output of each NAND gate is fed back to the input of the other gate. It has two inputs $\overline{R}$ and $\overline{S}$ and two outputs Q and $\overline{Q}$. These two outputs are complementary i.e. if Q = 1, $\overline{Q}$= 0 and if Q= 0, $\overline{Q}$= 1. It has two stable states i.e. Q=0 $\overline{Q}$= 1, and Q= 1, $\overline{Q}$ =0.Hence it is

called the bitable multi vibrator.

Let us now examine the output when fed by different combination of inputs.



27.1(a) RS Flip-Flop

(a) $\overline{S} = 0$ and $\overline{R} = 1$

NAND gate A has one of its inputs at logic 0. Hence its output Q must be at logic 1 (Remember the property of the NAND gate i.e. output of a NAND gate is 1 unless both inputs are 1s). Q is fed back to input of B and so both the inputs of the second gate are 1 s; hence its output $\overline{Q} = 0$. This is a stable state. It is called the "set "state.

If we now make $\overline{S} = 1$ with $\overline{R}$ still at 1 the inputs of gate A are 1 and 0 (since Q = 0). Since one of the inputs is zero, Q stays at 1, the circuit has thus remembered the last state Q = 1. Hence it can be used as a memory unit.

(b) $\overline{S} = 1$ and $\overline{R} = 0$

Since one of the inputs of NAND gate B is zero and its output is 1 i.e. $\overline{Q} = 1$. Since the inputs of gate A are 1, Q = 0. This is the other stable state. It is called the clear or "Reset" state.

If we now make $\overline{R} = 1$ with S still at 1, Q remains at 0.

(c) $\overline{S} = 1$ and $\overline{R} = 1$

Let us assume Q to be at 0 and $\overline{Q} = 1$ before application of the inputs. Since one of the inputs of the gate B is 0, its output is 1 (A = 1). As a result the inputs of gate A are both ones leading to the condition Q = 0. The previous output state is retained remembers the last state.

If $\overline{Q} = 1$ before the application of the inputs, the output of gate2 is 0 (Q:: 0) and Q becomes 1. Here again the previous state is retained.

(d) $\overline{S} = 0$ and $\overline{R} = 0$

In this condition we get Q = 1 and $\overline{Q} = 1$ This is not an allowed state. It only means Q

may be 1 and $\overline{Q} = 0$ or vice versa. We cannot predict the result. Hence this state is forbidden.

The truth table of this flip-flop is shown in Table 27.1

Table 27.1. Truth table of RS Flip-Flop

	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
State Set	0	1	1	0
	1	1	1	0
Reset	1	0	0	1
	1	1	0	1
	1	1	Q	Q
	0	0	Indeterminate or Forbidden state	

Since we have to apply inputs to $\overline{S}$ and $\overline{R}$ inputs of the Flip Flop we cannot directly apply S and R inputs. To overcome this difficults, two inverters are incorporated in each of the input terminals as shown fig 27.1 and then to S and inputs can be directly applied. These Flip Flops are also called latches as then Fig RS Flip Flop

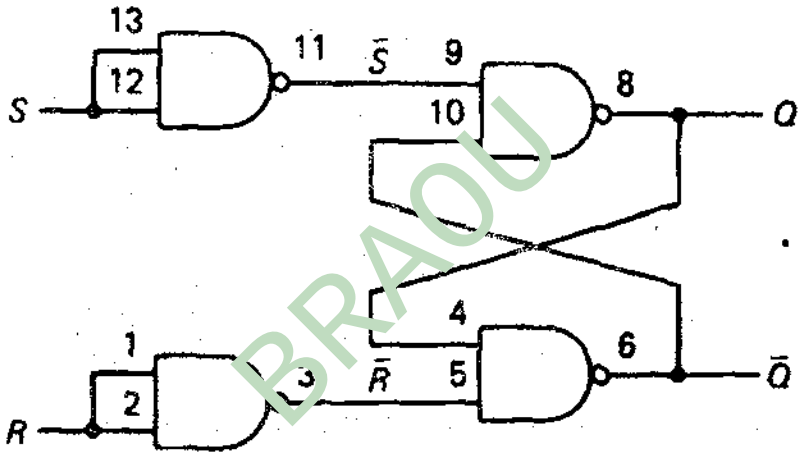


Fig 27.1(b) RS Flip – Flop (latch)

Truth Table

S	R	Q	$\overline{Q}$
0	0	Remembers Last State	Remembers Last State
1	0	1	0 Set
0	1	0	1 Reset
1	1	For bidden State (output Indeterminate)	

27.3 CLOCKED RS FLIP-FLOP

In some applications it becomes necessary to set or reset the RS Flip-Flop in synchronism with clock or trigger pulse. The RS flip-flop studied in the previous section can be modified into clocked RS flip-flop as shown in Fig. 27.2. It responds to the input data.

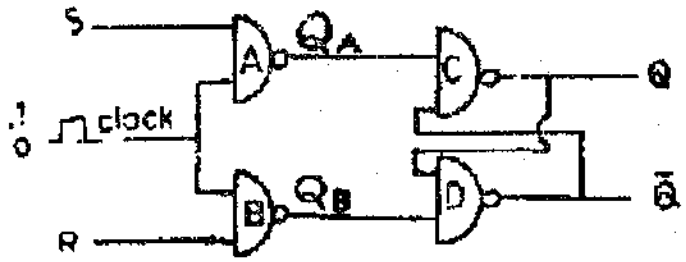


Fig. 27.2 Clocked RS Flip-Flop

When the clock input is zero, the output of each of the gates A and B is equal to 1 which disables the flip-flop. i.e. The outputs do not change (please refer to Table 31.1). When the clock is 1. If S = 1 and R = 0, $Q_C = 0$ and $Q_B = 1$, which in turn leads to Q = 1 and $\bar{Q} = 0$. i.e. the data given at the input passes to the output only when the clock input is at 1.

In a similar way use of the basic property of the NAND gate leads to the truth table showr in Table 27.2.

Table 27.2. Truth Table of Clocked RS Flip-Flop

R	S	Q^+
0	0	Q
0	1	1
1	0	0
1	1	Indeterminate (forbidden)

Q+ indicates the state of Q after the application of clock pulse.

27.4 D-FLIP FLOP

This RS Flip Flop has two data inputs Viz the S and R to store a high bit in Q we need to input S high and R low; to store a low bit Q we need to input S low and R high. Generation of two signals of opposite polarity is a major disadvantage. Further, the forbidden condition or both R and S being high may occur inadvertently since the inverter connected between the input A_1 and A_2 In order to overcome these two disadvantages D- Flip Flop has been designed which needs only a single data input this is shown in fig 27.3

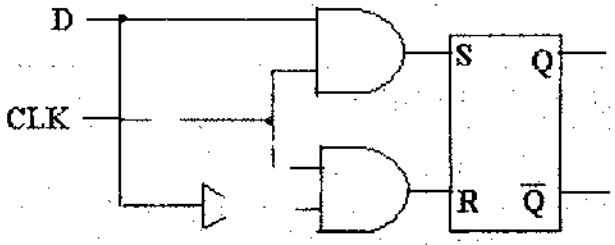
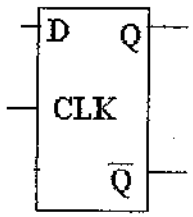


Fig. ... D Flip Flop

This kind of flip flop prevents the data present at D from reaching output Q until the clock pulse is high and enables both the AND gates A_1 and A_2. When the clock pulse is low the data will not be allowed to reach the output Q. Thus, Q retains or stores the last value of the data.

The logic symbol and Truth table are shown below



CLK	D	Q_{n+1}
0	X(don't Care)	Q_n (Retains Last State)
1	0	0
1	1	1

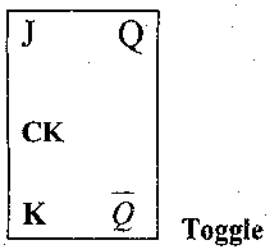
Logic symbol

Truth table

A four bit data storage scheme has been demonstrated using D – flip flop in fig 27.3. When the clock goes high, the four bits of input data D_3, D_2, D_1 and D_0 are loaded into the four D flip flop. When the clock goes low the data are retained. Thus the above 4 flip flop acts as 4 – bit data registers.

27.5 JK FLIP-FLOP

It is not possible to achieve toggling (changing the state of the output whenever the input makes a transition from 1 to 0) with the simple flip-flops described above. By using 8 NAND gates and a NOT gate one can construct a flip flop that toggles. The symbol and truth table of one such circuit, called JK Master-Slave flip-flop are shown in Fig. 27.4.



J	K	Q+
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

Toggle

(a) (b)

Fig. 27.4 (a) Symbol (b) Truth table

The output of this flip-flop changes state on downward transition of the clock pulse. An examination of the truth table given in Fig. 27.4 (b) reveals the following properties of the JK Flip-flop.

(a) It retains its present state if J = 0 and K = 0

(b) If J = 0, K = 1, Q = 0, it Resets to zero

(c) If J = 1, K = 0, Q = 1, it Sets
(d) If J = 1, K = 1, it Toggles.

If the first clock pulse leaves Q = 1 and $\overline{Q}$ = 0 the second clock pulse make Q = 0 and $\overline{Q}$ = 1. The third clock pulse make Q = 1 and $\overline{Q}$ = 0 again and so on as shown in Fig. 27.5

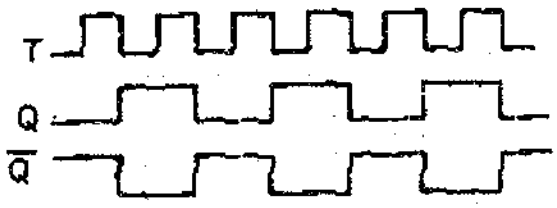


Fig. 27.5 Relation between Clock pulses and output JK Flip Flop.
When J = 1 and K =1

Please note Q = 1 once in every two clock pulses i.e. the output has half the frequency of the clock pulse. This property is utilized in binary counters.

27.6 BINARY COUNTER

Counters consist of a chain of flip-flops connected in such a way that they toggel when the pulses to be counted are given to their clock inputs, A two-bit binary counter is shown in Fig. 27.6. It consists of two cascaded toggling flip-flops FF-A and FF-B

The flip-flops are triggered by the trailing (falling) edge of a pulse. The J and K inputs of both flip flops are connected to logic level-I. The pulses to be counted are applied to the clock input of FF-A. The output of the first FF feeds the clock input to the second flip-flop. Each of these flip flops acts as a divide by two counters. The waveforms of the clock input, Q_A and Q_B are shown in Fig. 27.6.

We may use four flip-flops to divide the pulses by 16. In general, if there are n flip-flops the circuit divides the input pulses by 2^n.

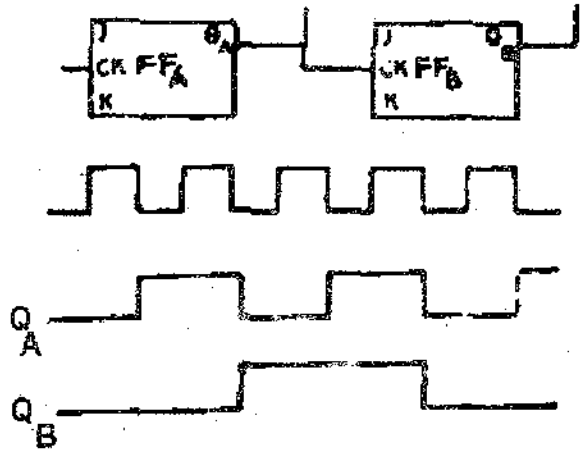


Fig. 27.6 (a) Divide:-by-4-Circuit (b) Wave: form

With these circuits it is possible to divide by 2, 4, 8, 16 etc. Since we are accustomed to decimal system, we may often need decade counters (divide by 10 circuits). Such a circuit consists of 4 flip-flops. It is connected in such a way that after 0, 1,2, 3,4,5,6, 1, 8 and 9 all the flip-flops are reset to 0. After this fresh counting starts.

27.7 SUMMARY

Flip Flops are also known as sequential logic circuits. Using the toggling property of the Flip Flop binary and decade Counters are constructed.

27. 8 MODEL EXAMINATION QUESTIONS

I. Answer the following questions in detail

1. Distinguish between R.S and JK flip-flops.

II. Answer the following questions briefly.

1. What is a combinational logic circuit? What is a sequential logic circuit? Explain
2. What are flip flops? Discuss the actions of an RS Flip-Flop.
3. Discuss the action of an RST flip-Flop.
4. What is a JK Flip-Flop? Explain its action.
5. Explain the working of a binary counter.
6. Explain the working of a decade counter.

27.9 REFERENCES

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UNIT – 28 FUNDAMENTALS OF MICROPROCSEEORS

Contents

28.0 AIMS AND OBJECTIVES

This unit introduces you to the field of microprocessors in general with a particular Bias on Intel 8085 microprocessor. This chapter provides you with the basic background knowledge about microprocessors.

28.1 INTRODUCTION

The developments in the field of Microprocessor are taking place at a tremendous pace with the developments in the field of computers and in automation. Hence it is essential for the student of electronics to be acquainted with the subject of Microprocessors.

28.2 MICROPROCESSORS

Microprocessor is the part of a digital computer just as the operational amplifier is for an analog computer. The term microprocessor is abbreviated a μ P. It is a powerful tool in the fields of Science and Technology. It can be used for data acquisition, data processing, data storage and for control operations etc. Interfacing the μ P with several input/output devices and memory units can be programmed to carryout all these tasks. The μ P can be built in to computer and interfaced with any scientific equipment or industrial units for the measurements and control of instruments in the research laboratories industrial processors ete.

28.3 EVOLUTION OF MICROPROCESSORS

With the developments in the field of very large scale integration (VLSI) techniques, it was made possible to design a microprocessor-integrated chip. The first microprocessor 4004 was introduced by Intel Corporation in 1971 into the industry and later on an enhanced version of the earlier μ P namely 4040 was introduced by the same Intel Corporation. Both these μ P are 4-bit processors, which were a great success in industry. This as followed by another 4 – bit processor MS1000 from Texas Instruments.

The first 8-bit microprocessor, which could perform arithmetic and logic operations on 8-bit words, was introduced in 1973, again by Intel. This was the 80[illegible]8 that was followed by an improved version— the 8080 from the same company. Today there are a variety of 8-bit processors, some examples being Motorola's M6800, National Semiconductors' SC/MP, Zilog Corporation's Z80, Fairchild's F8, Intel's 8085, and Hitachi's 6809.

The 8-bit microprocessor was followed by [illegible]processors operating on 12-[illegible] 16-bit data words, respectively. Intersil's IM6100 and Toshiba's T3190 are examples of 12-bit processors. Examples of 16-bit microprocessors are Fairchild's 9440, Data General's mN 601 and Texas Instrument's TMS9900. Intel's 8086 and 80286, Motorola's M68000 and Zilog's Z8000 are some of the most powerful 16-bit microprocessors available today.

One of the most popular 16-bit μ Ps has been the 8088 from Intel. The 8088 has the same instruction set as the 8086. However, it has only an 8-bit data bus. The 8088 is the μ P used in the IBM PC and its clones. The new IBM P5/2 series personal computers use the 8086, 80286, and 80386, 80486 and Pentium – I, II, III, IV.

The latest in this sequence are the 32-bit microprocessors introduced by several companies. Intel's iAPX 432, Hewlett Packard's HP32 are two examples of the earlier 32-bit P's. The iAPX432 is now extinct. Intel now offers the 80386, which is a very powerful 32-bit μ P. It also forms the basis of many advanced personal computers and workstations. Motorola's 68020 and 68030, National's 32032 and 32523, Inmos' T414 and T800, are a few other widely used 32-bit pP s.

At present, microprocessors are available from many manufacturers. Examples of widely used microprocessors include the Intel 8080A and 8085, Zilog Z80, Motorola 6800 and 6809, and MOS Technology 6500 series. Microcomputers such as the Radio Shack TRS-80 and the Tele Video 802 are designed around the Z80 microprocessor. The design of the IBM Personal Computer is based on the Intel 8088 microprocessor. Single-bc rd microcomputers such as the Intel SDK-85 (see Figure 1.5), the Motorola MEK-6800-D2, and the Rockwell Aim 65 are commonly used in college laboratories. The SDK-85 is based on the 8085 microprocessor, the MEX-6800-D2 is based on the 6800 microprocessor, and the Aim 65 is based on the 6502 microprocessor.

Presently, the highest performing Pentium-IV with a clock speed of 2.4 GHz and memory address capability of 2^{32} bits is in use.

28.4 ORGANISATION OF MICROPROCESSOR

A microprocessor if interfaced with several Input/Output (I/O) devices and memories becomes a microcomputer it is also known as the Central Processing Unit (CPU) in large computers. The organisation of a microprocessor in microcomputer is shown in the following figures 28.1 and 28.2.

Here, we take a quick look at a μP. A μP is just like any other electronic chip. However, it is more powerful than just any other chip. For the present, we can consider a μP to be a device that is programmable logic device

- has a limited set of on-chip memory locations, known as registers, to hold information,
- can understand a fixed set of basic commands, and
- can generate signals to control external devices.

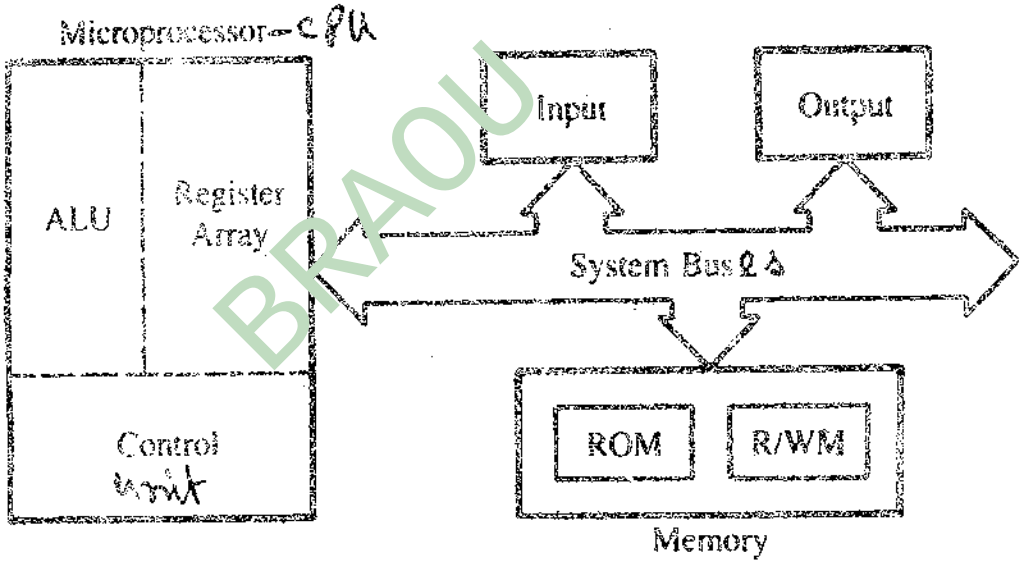


Fig. 28.1 Block Diagram a Microcomputer

There is an arithmetic logic unit (ALU) Inside the chip. The ALU executes all arithmetic and logic instructions. For example, the arithmetic addition and logical AND operations will be performed by the ALU. The registers inside the P hold data on which the operations are performed. The control unit generates the external control signals and also controls the operation of the internal on-chip circuitry.

The on-chip memory, in the form of registers, is generally very limited. Thus, almost every μP based system has an off-chip memory also.

The set of basic commands that a μP can understand, is known as the instruction set of the μP.

Fig. 28.2 shows the pin configuration and the signals available on 8085 μP chip. The

chip itself has several pins, like any other chip. The μ P sends or receives information over these pins. Sometimes we refer to the connections between the pins, or the pins themselves, as lines. Each pin transmits or receives a boolean signal which is either at logical 0 or at logical 1. Some pins may be in neither of these two states at certain points in time. Such pins, or lines, are said to be tn-state outputs.

28.4.1 Address Bus:

As shown in Fig. 1.1, a typical μ P has several lines over which it transmits an address to the off-chip memory or to the I/O devices. These are referred to as address lines. More often, the address lines are known as the address bus. A typical 8-bit μ P will have an address bus consisting of 16 lines for transmitting the address. Thus, such a μ P can transmit an address that is 16-bits wide. How many different addresses can be transmitted? A knowledge of the binary number systems tells us that in all $2^{16} = 65386$ different addresses cair be transmitted.

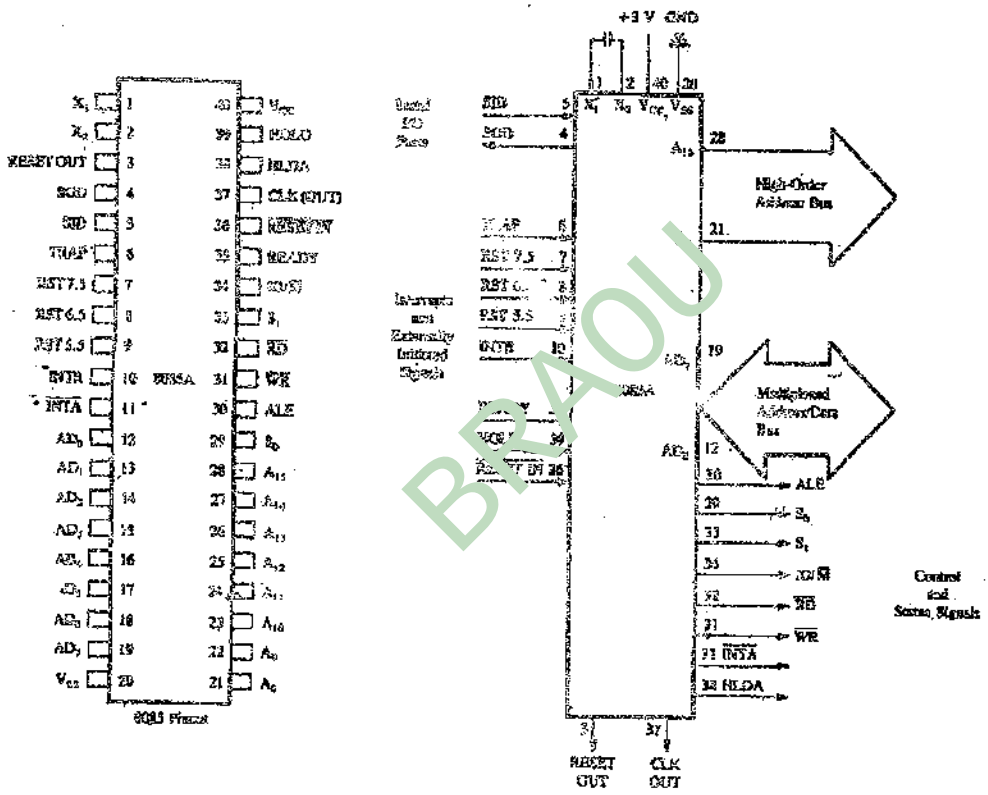


Fig 28.2 Shows the pin configuration and Signals Available on them

28.4.2 Data Bus:

Every μ P has a set of lines for transmitting and receiving data. These lines are referred to as the data bus. An 8-bit μ P will generally have eight-lines in its data bus. A 16-bit μ P may have either 16 lines in its data bus, or only eight-lines. For example, the 8085 μ P from Intel is an 8-bit μ P and has eight-lines in its data bus. The 8086 μ P, also from Intel, has 16-lines in its data bus and is a 16-bit μ P. However, the 8088, again from Intel, is a 16-bit μ P but has only eight-lines in its data bus. A lesser number of data bus lines are provided to reduce the space required on a printed circuit board for the data bus lines. In a later section we shall learn what we mean by saying that a μ P is an 8-bit or a 16-bit μ P.

28.4.3 Control Bus:

A μP also has lines for controlling the input and output devices. These devices could be an electric motor, or a display lamp or one of a variety of other devices that we shall mention in the remainder of this book.

In addition to the control signals for input/output devices, a μP also has some other control signals for (a) controlling off-chip memory, (b) providing information about its own status and (c) performing other miscellaneous tasks.

The microprocessor is a semiconductor device consisting of electronic logic circuits manufactured by using very-large-scale integration (VLSI) technique. The microprocessor is capable of performing computing functions and making decisions to change the sequence of program execution. In large computers, the CPU performs these computing functions and it is implemented on one or more circuit boards. The microprocessor is in many ways similar to the CPU; however, the microprocessor includes all the logic circuitry (including the control unit) on one chip. For clarity, the microprocessor can be divided into three segments, as shown in Figure 28.2 arithmetic/logic unit (ALU), register unit, and control unit.

ALU:
Arithmetic/Logic Unit. In this area of the microprocessor, computing functions are performed on data. The ALU performs arithmetic operations such as addition and subtraction, and logic operations such as AND, OR, and exclusive OR. Results are stored either in registers or in memory or sent to output devices.
l Register Unit: This area of the microprocessor consists of various registers. The registers are used primarily to store data temporarily during the execution of a program. Some of the registers are accessible to the user through instructions.
Control Unit: The control unit provides the necessary timing and control signals to all the operations in the microcomputer. It controls the flow of data between the microprocessor and peripherals (including memory).

At the outset, we will differentiate between the terms microprocessor and microcomputer because of the common misuse of these terms in popular literature. The microprocessor is one component of the microcomputer. On the other hand, the microcomputer is a complete computer similar to any other computer, except that the CPU functions of the microcomputer are performed by the microprocessor. Similarly, the term peripheral is used for input/output devices; however, occasionally memory is also included in this term. The various components of the microcomputer shown in Figures 28.2 and 28.5 and their functions are described in the following paragraphs.

INPUT:

The input section transfers data and instructions in binary form the outside world to the microprocessor. It includes devices such as keyboards, teletypes, and analog-to-digital converters. Typically, a microcomputer used in college laboratories includes either a hexadecimal keyboard oran ASCII keyboard as an input device. The hexadecimal keyboard has sixteen datA keys (0. to 9 and A to F) and some additional function keys to perform operations such as storing data and executing programs. The ASCII keyboard is similar to a typewriter keyboard, and it is used to enter programs in an English-like language. Although die ASCII keyboard is found in most microcomputers, single-boud microcomputers generally have a Hex keyboard.

OUTPUT:

The output section transfers data from the microprocessor to output devices such as light emitting diodes (LEDs), cathode-ray-tubes (CRTs), printers,, magnetic tape, or another computer. Typically, single-board computers include LEDs and seven-segment

LEDs as output devices.

MEMQRY:

Memory stores binary information such as instructions and data, and provides that information to the microprocessor whenever necessary. To execute programs, the microprocessor reads instructions and data from memory and performs the computing operations in its ALU section. Results are either transferred to the output section for display or stored in memory for later use. The memory block (Figure 28.1 and 2) has two sections: Read-Only Memory (ROM) and Read/Write Memory (RIWM), popularly known as Random-Access Memory (RAM).

RAM:

The ROM is used to store programs that do not need alterations. The monitor program of a single-board microcomputer is generally stored in the ROM. This program Interprets the information entered through a keyboard and provides equivalent binary digits to the microprocessor. Programs stored in the ROM can only be read; they cannot be altered.

ROM:

The Read/Write memory (R/WM) is also known as user memory. It is used to store user programs and data. In single-board microcomputers, in which instructions and data aie entered through a Hex keyboard, the monitor program monitors the keys and atom those instructions and data in the RIW memory. The information stored in this memory can be read and altered easily.

SYSTEM BUS:

The system bus is a communication path between the microprocessor and the peripherals; it is nothing but a groupof wires that carries bits. (In fact, there are several buses in the system; we will discuss them in the next chapter.) The microcomputer bus is in many ways similar to a one-track, express subway: the bus carries bits, just as the subway carries people. The analogy of an express subway with only one destination is more appropriate than that of a regular subway, because the microcomputer bus carries bits between the microprocessor and only one peripheral at a time. The same bus is time-shared to communicate with various peripherals, with the timing provided by the control section of the microprocessor.

28.5 INSTRUCTIONS/ LANGUAGES/PROGRAMMING

28.5.1 Machine Languages:

Each microprocessor has a unique set of machine language instruction defined by the manufacturer. Each instruction in machine language normally consists of a string of 1's and 0's. It is very inconvenient for the programmer to remember all these instruction in machine language. In order to improve the programmers efficiency in writing in machine language programmes Hexa decimal numbers rather than binary numbers are used for instructions. It is relatively easier to detect errors in Hexa decimal digits rathe than skins of binary number running up to 32 to 64. Further these machine language instruction are not common to all microprocessors.

Some of the machine language instructions and their corresponding Hexa decimal representation are presented in table 28.1.

Table28.1

Machine language Code	Hexadecimal Code
0111 1110	3E
0001 0000	10
1100 0110	C6
0010 0000	20
0010 0001	21
0000 0000	00
0000 0010	02
0111 0110	77

28.5.2 Assembly Language:

Since the machine language programming is very inconvenient, and difficult to memorize an assembly language program is developed which consists of certain mnemonics (Symbolic codes) which are very close to the English language word and convey the idea of the type of operation the UP is suppose to perform. The translation of the operation codes (Op. Codes) into machine languages in Hexa Decimal form is done either directly by the programmer with the help of a set instruction set along with the corresponding Op. Codes Hexadecimal numbers or can also be carried by an assembler. Assembler is also a program which is stores in the memory of automatically translates theses mnemonics into op codes as shown by the following Fig.28.3

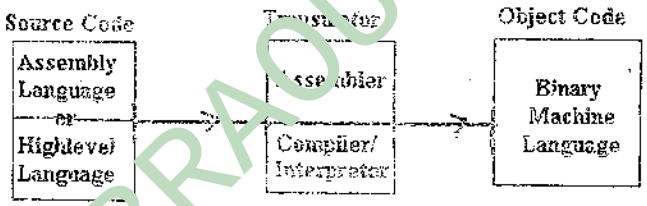


Fig. 28.3

28.5.3 High Level languages:

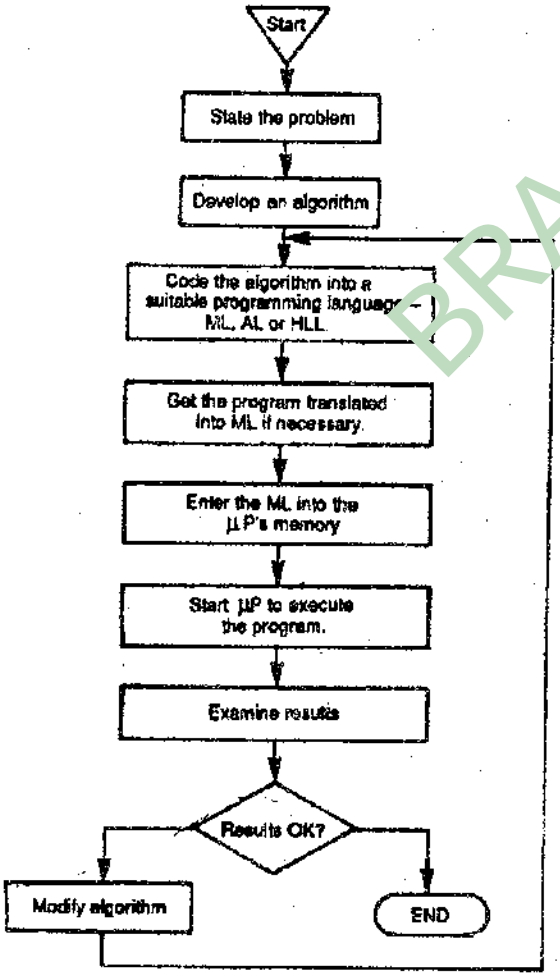
Even though the programmer's efficiency improves slightly with programming in assembly language compared to machine language programming. However, the programmer should be acquainted with the architecture and the instruction set of each microprocessor, which is again a very difficult task. An example for adding two numbers using assembly language programming is shown in the following table 28.2

Table 28.2

Assembly Code	Binary form of ASCII codes as Seen by Assembler	Binary Op. Codes Created by Assembler
H	0100 1000	
L	0100 1100	0111 0110
T	0101 0100	

Label	Mnemonic	Operand		Comment
START	MVI	A, 10H	;	Move 10_{16} into accumulator
	ADI	20H	;	Add 20_{16} to contents of accumulator
	LXI	H, 0200H	;	Load register pair with 0200_{16}
	MOV	M, A	;	Move contents of accumulator into location 0200_{16}
	JMP	START		Jump to beginning of program

It is a very tedious process for the programmer to write all these steps for a simple addition. Hence high-level languages like BASIC, FORTRAN, COBOL, and C etc have been developed. In which the programming becomes very simple. A single instruction in high-level language corresponds to a set of instruction in assembly or machine language. In order to translate instruction in high-level language into the machine language translators or interpreter known as compilers are developed for each of these languages. The compilers are nothing but software programs the high level languages. These high level languages are machine independent which is a highly advantages feature.



28.5.4 Programming of Microprocessor

The total instruction set of microprocessor 8085 are classified into five groups namely the

(i) Data Transfer Group
(ii) Arithmetic Group
(iii) Logical Group
(iv) Branching Group
(v) Stack, I/O and machine control.

Fig 28.4 The programming flow chart for the programming process

The programming sequence to be followed to solve any problem can be specified in the following sequence of step

(i) Data Transfer Group:

1. State the problem clearly.
2. Develop the algorithm in the best possible way.
3. Prepare a flow chart
4. Test for any logical or Syntactic errors and rectify
5. Run the program

The sequence of these steps can be represented in a flow chart shown in fig. 28.4

28.6 ARCHITECTURE OF μP 8085

The functional block diagram of the 8085 microprocessor is shown in fig 28.5

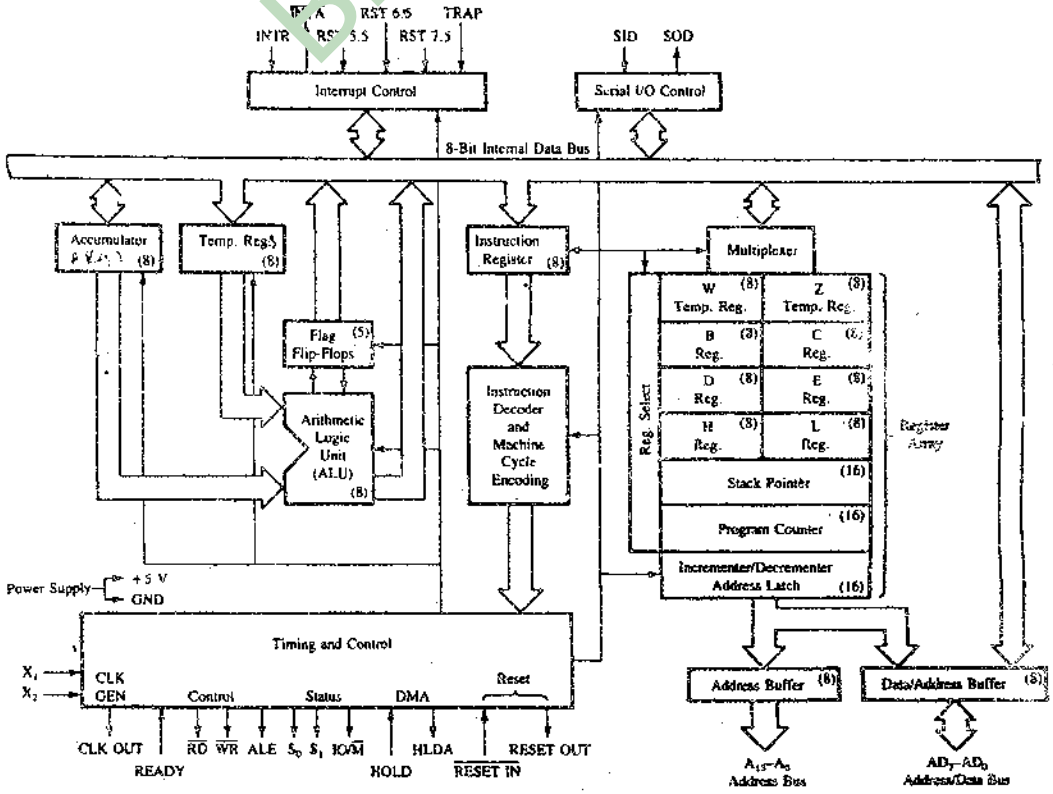


Fig. 28.5 Architecture of microprocessor 8085

28.6.1 Data and Address Busses

The 8085 is, an 8-bit microprocessor available as a 40-lead plastic ceramic package. The data bus is 8 bits wide ($D_7 - D_0$). This implies that 8 bits (1 byte) of data can b6transferred to or from the 8085 in parallel. There are eight pins dedicated to transmit the most significant 8 bits of the memory address. The least significant 8 bits of the same address are transmitted on the eight lines on which data are also transmitted ($A_{D7} - A_{D0}$). Thus, data and part of the address are transmitted over a set of shared lines. This is known as address multiplexing. It is obvious that the data and address (least significant 8 bits) are transmitted at different points in time. Due to this multiplexing, the 8085 bus is also referred to as multiplexed bus. The most significant 8 bits are sent on address lines ($A_{15} - A_8$).

Thus, the 8085 has a 16-bit address transmission capability. This implies that a total of 2'~ (=65536) memory locations can be addressed directly by 8085. Each location is a byte as 8 bits of data is transferred in parallel between the 8085 and the memory. Therefore, we say that the 8085 can directly address 64K (1 K = 1024) bytes of memory.

28.6.2 Addressing the I/O Devices

In any microcomputer, the μ P will be connected to the memory as well as to I/O devices. We have seen earlier how a μ P addresses any memory location. It is possible to design a pG in such a way that an input or an output device is treated by the μ P as one memory location. Thus, for example, address 5 may correspond to a LED display and 6 to a keyboard. This would mean that no byte in the memory would have an address 5 or 6. This form of connecting I/O devices to a μ P is known as memory mapped I/O.

However, it is also possible to treat I/O devices as distinct from the memory and assign them addresses that do not conflict with the memory addresses. According this scheme, an address such as 5 could be the address of a memory location as well as an I/O device. This scheme is known as I/O mapped I/O.

When the I/O mapped I/O scheme is used, an address on the address bus may refer either to a memory location or to an I/O device. In order that the memory and the I/O devices be able to decide which one the address is meant for, the μ P (see Fig. 3.1) issues another signal on the IO/i~T line. If this line is high (i.e. logical 1) then the address is meant for an I/O device, otherwise it is for the memory. However, the address for any input or output device can be in the range 0 to 255. Thus, the memory and I/O devices may use this line to decide for whom the address on the address bus is meant.

28.6.3 Registers in the 8085

Inside the 8085 there are several registers used during the execution of a program. We shall now describe the size and use of each of these registers. Fig. 28.4 may be referred to while reading about these registers.

There is one 8-bit register known as the Accumulator (abbreviated as ACC). It is used for various arithmetic and logical operations. For example, during the addition of two 8-bit integers, one of the operands must be in the accumulator. The other may be either in the memory or in one of the other registers.

There are six general-purpose 8-bit registers that can be used by a programmer for a variety of purposes. These registers are labeled as B, C, D, E, H, and L. They can be used individually, such as when operation on 8-bit data is desired, or in pairs such as BC,DE, HL

when a 16-bit address is to be stored. When used in pairs, only the combinations shown in Table 3.1 are permitted. The codes mentioned in this table are used to refer to a register pair in an instruction as explained later in this chapter. These registers can be referred to individually using codes given in Table 3.2. The codes mentioned in Tables 3.1 and 3.2 are needed only when writing a machine language program.

There is a 16-bit register, which is used by the 8085 to keep track of the address of the instruction in the memory that has to be executed next.

This register is called program counter, abbreviated as PC. The contents of the program counter are automatically updated by the 8085 during the execution of an instruction so that at the end of execution of this instruction it points to the address of the next instruction in the memory. Recall that 16 bits of address are sent out by the 8085 on the address bus. In some instances, the PC holds this address before it is transmitted.

There is another 16-bit register, known as stack pointer, abbreviated as SP. It is used by the programmer to maintain a stack in the memory. More about the stack and SP will be explained later in this chapter. A set of five flip-flops, 1-bit registers, serve as flags. These registers indicate certain conditions such as overflow or carry that arise during arithmetic and logical operations. The function of each of these registers, and condition flags is explained later.

Several other registers shown in Fig. 3.2 are used by the 8085 only for its internal operation. They cannot be accessed by the programmer. Hence, we shall not explain their function in this chapter.

Table 28.3(a)	
Register	Code
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Table 28.3(b)	
Register	Code
B – C	00
D – E	01
H – L	10
SP	11

28.7 APPLICATIONS OF MICROPROCESSOR

The microprocessor finds extensive applications in the laboratories and industries for measurement and control of various parameters and processes; in defence for the control of defence radars missiles and several other equipments; in Bio-Medical fields for the automatic patient monitoring systems, scanners, and in intensive care units etc.; even in home appliances like microwave ovens, washing machines, television sets CD-Players, musical equipment, music synthesizes; Desktop publishing; data acquisition;

28.8 SUMMARY

In this unit type of microprocessor Evaluation of microprocessors organisation of microprocessor architectural features and applications of microprocessor have been studied. This chapter provides the basic background knowledge about the microprocessors and their programming languages etc.

28.9 MODEL EXAMINATION QUESTIONS

I. Answer the following questions briefly.

1. What are the functional blocks in μ P 8085?
2. What are the functions of each block of a microprocessors?
3. What is the role of a microprocessor in a microcomputer?
4. What is the central processing unit?
5. Name the blocks in CPU and explain the goals.
6. Explain the terms machine language, Mnemonic, assembly?
7. Estimate the number of memory locations that can be addressed by a 16-bit microprocessors?
8. Explain the terms algorithm, flow chart?

MODEL PROBLEMS

It is desired to add the number 5 to the contents of memory location OAB12H and store the result in location OFAOFH. Assuming that the symbolic address for OAB12H is Z, we may use the following instruction sequence to perform this task.

```
LXI H, OFAOFH      ; Load register pair H-L with OFAOFH.
LDA   Z            ; Get value of Z in AGO.
ADI   5            ;Add 5 to it      (3.7)
MOV   M, A         ; Store AGO in memory location
                     Pointed to by register pair H-L (i.e. to
                          location OFAOFH)
```

In (3.7), first we use an LXI instruction to put the address OFAOFH in register pair H-L. The next three instructions in (3.7) fetch the desired contents, add 5 to it, and store the sum in location OFAOFH using the MOY instruction. The MOV instruction in (3.7) uses register indirect addressing. We may write (3.7) in machine language as:

```
00100001000011111 11111010  ;    LXI H, OFFAH
00111010000010010 10101011  ;    LDA Z (3.8)
11000011000000101           ;    ADI 5
01110111                    ;    MOV M, A
```

Note that instructions using immediate addressing may be 2 or 3 bytes long.

Implicit Addressing

There are certain instructions that operate only on one operand. Such instructions assume that the operand is in the ACC and therefore require no address specification. Many instructions in the logical group like RLG, RRC, and OMA fall into this category. All these are 1 byte instructions. You may observe that those instructions that specify the address of one of the operands using one mode or the other, use implicit addressing for the other operand.

Example 3.5

it is desired to complement the contents of memory location 599211. This may be done by the following instruction sequence given below.

```
LXI    H, 5992H    ; Set H-L to point to location 5992H.
MOV    A,M         ; Get contents of 5992H in AGO.
OMA                ;Gomplement AGO                    (3.9)
MOV    M, A        ; Store the complement back
                   in location 5992H.
```

As mentioned earlier, there are several other addressing modes used in microprocessors. Some of these are introduced in section 3.8.2. As we shall see in the next section, the addressing modes aid the programmer in specifying operand addresses. A rich variety of these provides more flexibility to the programmer.

28.10 REFERENCES

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28.11 Glossary

Microprocessor	: It is an integrated which contains limited set of on-chip memory locations known as registers
Registers	: Electronic circuit(Flip-Flops) which digital Information
ALU	: Arithmetic logic unit in which all the arithmetical and logical operation are carried out
CPU	: Central Processing Unit of large computer which also contains same blocks as the microprocessors
RAM	: Random Access Memory, It's a temporary memory available to the user
ROM	: Read Only Memory in to which several machine programs etc are loaded
Accumulator	: it is known as Register – (a) where all the arithmetical operations carried out

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B.Sc. THIRD YEAR (3 YEARS DEGREE COURSE) EXAMINATION

MODEL QUESTION PAPER
PHYSICS
COURSE IV: ELECTRONICS

Time: 3 Hours Max. Marks: 70

SECTION-A

Note: Answer any THREE of the following

Each question carries 15 marks

Answer the following in about 30 lines.

1. Explain the formation of a barrier when p and n type semiconductors are joined together.
2. Explain the effect of negative feedback on the gain, band with, distortion of a an amplifiers.
3. Give the circuit diagram of a 3-pin voltage regulator.
4. Give the circuit diagram of a Full-adder, and explain its working.
5. Give the truth tables of the following gates
   NOR, NAND and XOR
6. Give the architectural diagram of a µP 8085 and explain its working.

SECTION-B

Answer any FIVE of the following questions in about 10 lines each.

Each question carries 5 marks.

7. Derive the Hybrid equivalent circuit of a transistor in CE configuration and estimate the parameters.
8. Derive expression for the gain of an Op .amp in inverting configuration.
9. Give a circuit diagram of Wein-bridge oscillator and derive expressions for the frequency of oscillation and the necessary condition for maintenance of oscillations.
10. Give the circuit diagram and derive expression for the time period of an a stable multivibrator.
11. Give the architectural diagram of µP8085 and explain.
12. Give the circuits diagram of an electronic series voltage regulator and explain its working.
13. Explain the working of a balanced differential amplifier type of electronic voltmeter.
14. Give the theory of amplitude modulation and derive expression for the out put of an amplitude-modulated wave.
15. Give the block diagram of a monochrome TV Transmitter and explain the function of each block.
16. Give the block diagram of SMPS and explain its working.

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UNDERGRADUATE COURSE-III

SUBJECT : PHYSICS

COURSE IV : ELECTRONICS

ASSIGMENT-1

NOTE :

1 Do not copy the answer directly from any of the books.

2 As far as possible try to answer the question independently in your own words

3 It is necessary to quote from any source, give the correct reference

4 Use your own full scape pages for writing the assignment

5 Leave sufficient margin for the comments of the evaluators

6 Completion of this assignment normally should not take more than 1 hour's time.

PART-A

I Answer the following questions in about 30 lines each.

1. Give the drain characteristic curves of a FET. How do you determine the drain resistance $-r_d$ from them.
2. What is the role of a filter in a rectifier circuits.
3. What is the necessary condition for maintenance of oscillations in a phase –shift oscillator?

PART-B

II Answer the following questions in about 10 lines each

1. Explain the mechanism of Zener break down
2. Explain the common mode rejection ratio in an Op. amp. give the formula for estimating the same
3. Explain the method of determining the phase difference between two sine waves of the same frequency.

Dr.B.R. Ambedkar Open University

UNDERGRADUATE COURSE-III

SUBJECT : PHYSICS

COURSE IV : ELECTRONICS

ASSIGMENT-2

NOTE :

7 Do not copy the answer directly from any of the books.

8 As far as possible try to answer the question independently in your own words

9 It is necessary to quote from any source, give the correct reference

10 Use your own full scape pages for writing the assignment

11 Leave sufficient margin for the comments of the evaluators

12 Completion of this assignment normally should not take more than 1 hour's time.

PART-A

I Answer the following questions in about 30 lines each

1. What is a microprocessor?

2 State the Boolean laws of communication, association.

3. Give the block diagram of CPU .

PART-B

II Answer the following questions in about 10 lines each

1 Give the diagram of amplitude modulated wave form

2. Give an expression for the modulation index in an FM

3. Explain the working of a JK Flip-Flop